

RELIABILITY REPORT
FOR
MAX667xxA
PLASTIC ENCAPSULATED DEVICES

August 28, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Conclusion

The MAX667 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX667 low-dropout, positive, linear voltage regulator supplies up to 250mA of output current. With no load, it has a typical quiescent current of 20 μ A. At 200mA of output current, the input/output voltage differential is typically 150mV. Other features include a low-voltage detector to indicate power failure, as well as early-warning and low-dropout detectors to indicate an imminent loss of output voltage regulation. A shutdown control disables the output and puts the circuit into a low quiescent-current mode.

The MAX667 employs Dual Mode™ operation. One mode uses internally trimmed feedback resistors to produce +5V. In the other mode, the output may be varied from +1.3V to +16V by connecting two external resistors.

The MAX667 is a pin-compatible upgrade to the MAX666 in most applications where the input voltages are above +3.5V. Choose the MAX667 when high output currents and/or low dropout voltages are desired, as well as for improved performance at higher temperatures.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Input Supply Voltage	+18V
Output Short Circuited to Ground	1sec
LBO Output Sink Current	50mA
LBO Output Voltage	GND to V _{OUT}
SHDN Input Voltage	-0.3V to (V _{IN} + 0.3V)
Input Voltages LBI, SET	-0.3V to (V _{IN} -1.0V)
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
8 Lead SO	471mW
8 Lead PDIP	727mW
Derates above +70°C	
8 Lead SO	5.88mW/°C
8 Lead PDIP	9.09mW/°C

II. Manufacturing Information

- A. Description/Function: +5V/Programmable Low-Dropout Voltage Regulator
- B. Process: Standard 6 micron metal gate CMOS
- C. Number of Device Transistors: 77
- D. Fabrication Location: California, USA
- E. Assembly Location: Philippines, Malaysia, Thailand or Korea
- F. Date of Initial Production: August, 1990

III. Packaging Information

A. Package Type:	8 Lead SO	8 Lead PDIP
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-0701-0393	# 05-0701-0629
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

- A. Dimensions: 70 x 111 mils
- B. Passivation: SiN/SiO (nitride/oxide)
- C. Interconnect: Aluminum/Si (Si = 1%)
- D. Backside Metallization: None
- E. Minimum Metal Width: 6 microns (as drawn)
- F. Minimum Metal Spacing: 6 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric: SiO₂
- I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Director)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 100 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{4.04}{192 \times 4389 \times 240 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

△
Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 9.98 \times 10^{-9}$$

$$\lambda = 9.98 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-1804) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1L**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PS22 die type has been found to have all pins able to withstand a transient pulse of $\pm 2500\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$ and/or $\pm 20\text{V}$.

Table 1
Reliability Evaluation Test Results
MAX667xxA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		240	1
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 96hrs.	DC Parameters & functionality	NSO	40	0
			DIP	60	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality (generic test vehicle)		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters (generic test vehicle)		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the Small Outline package.

Note 2: Generic package/process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} <u>3/</u>	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

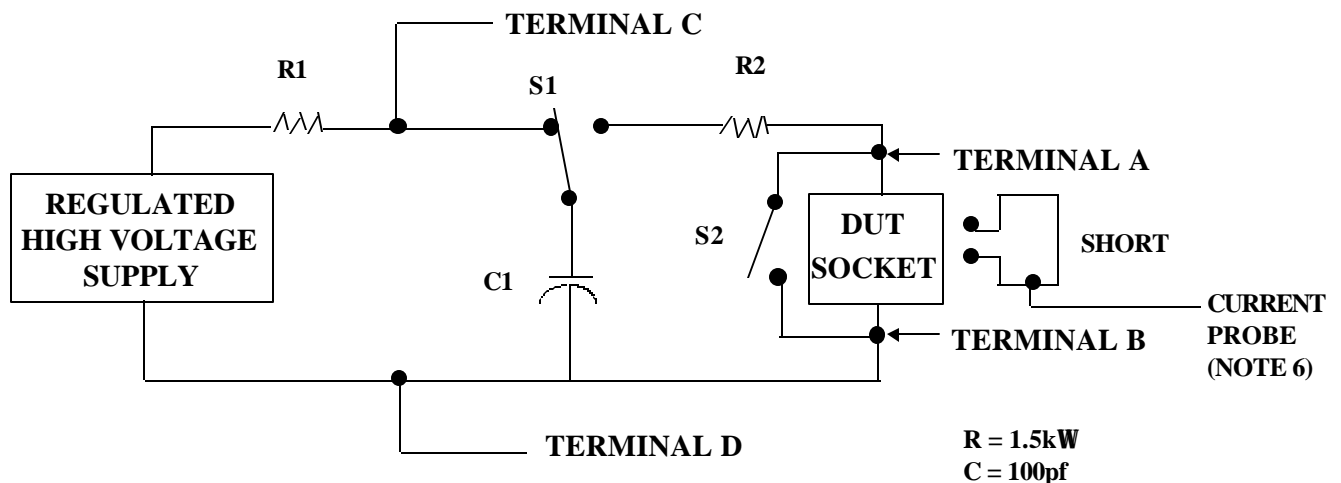
1/ Table II is restated in narrative form in 3.4 below.

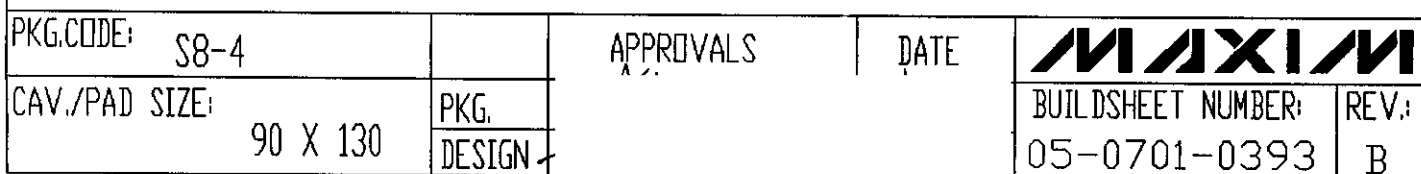
2/ No connects are not to be tested.

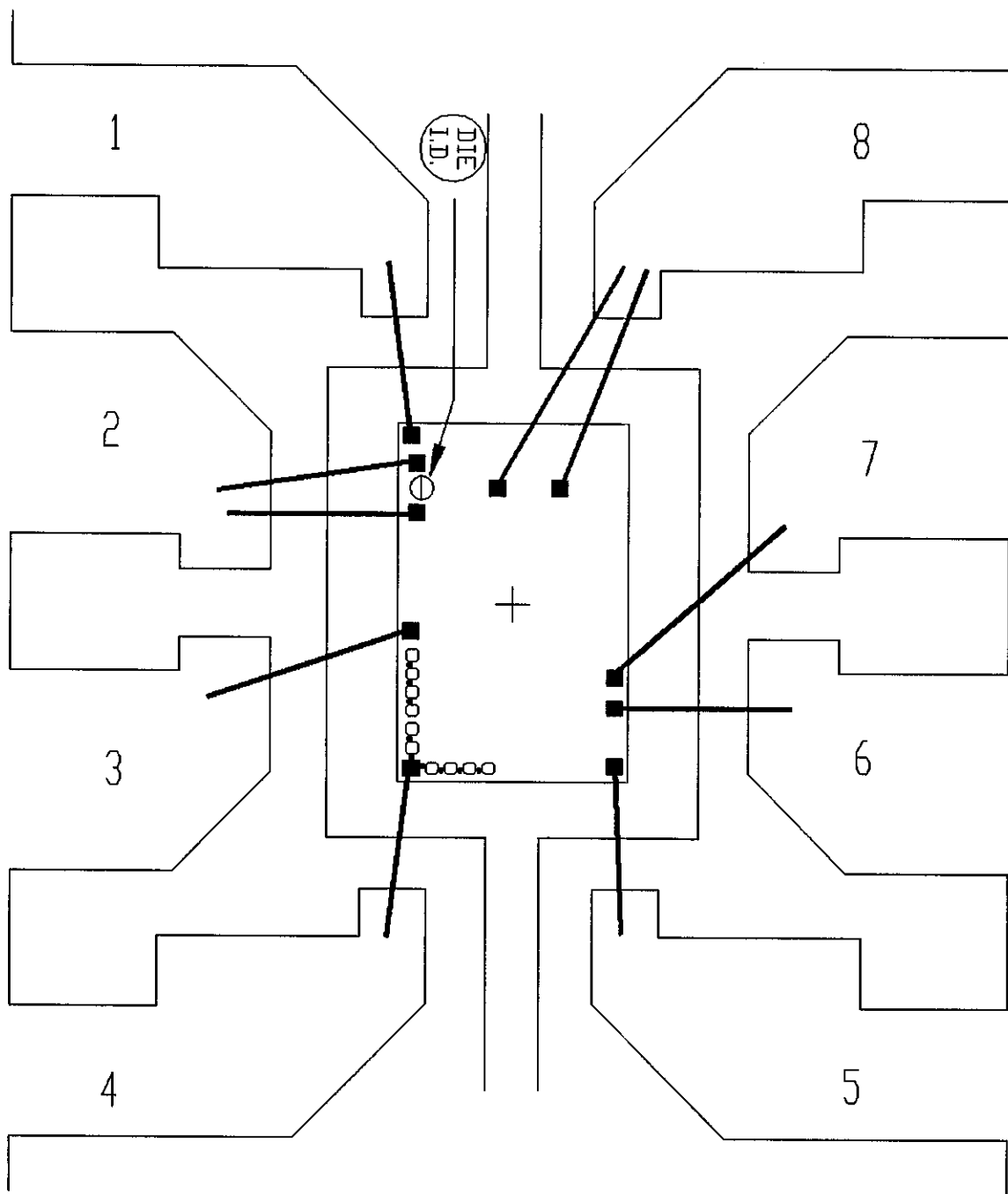
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).


3.4 Pin combinations to be tested.

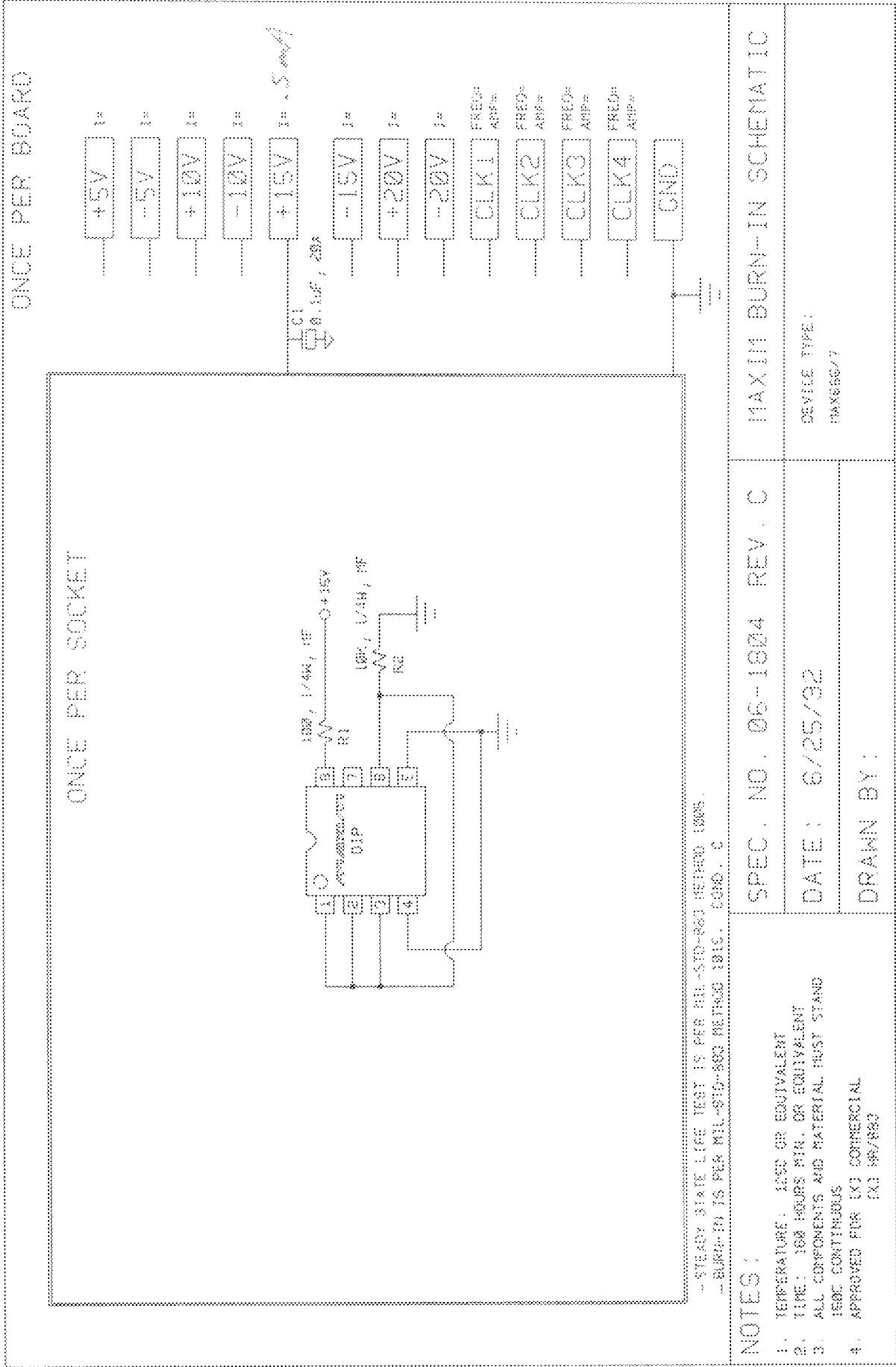
- Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.







PKG.CODE: P8-2		APPROVALS	DATE		
CAV./PAD SIZE: 110 X 140	PKG.			BUILDSHEET NUMBER:	REV:
	DESIGN			05-0701-0629	B



SPEC. NO. 06-1804 REV. C

MAXIM BURN-IN SCHEMATIC

DATE: 6/25/92

DEVICETYPE:
MAX5677

DRAWN BY: