APPLICATIONS AND OPERATION OF OPTOLOGIC ™

INTRODUCTION

Since the introduction of the optically coupled isolator, digital design engineers have struggled with the problem of achieving logic-in to logic-out compatibility over temperature, minimizing the effects of LED degradation, and obtaining high speed operation. Typically this problem is approached by selecting input/output resistors, and often by trial and error.

This guesswork type of interfacing is now a thing of the past. Enter the New Optologic™ family of logic-to-logic compatible, optically coupled isolators. This easy to use logic element offers LSTTL-in to TTL-out or LSTTL-in to CMOS-out. The device eliminates the resistor selection and features guaranteed DC parameters over temperature.

This ease of design-in and operation is made possible through the use of an input amplifier that provides the interface between the driving LSTTL gate and the LED emitter. The output circuitry consists of a multistage high speed amplifier available with either a totem pole or open collector output. The input amplifier, LED, and output amplifier are assembled in an industry standard six pin package.

The Optologic devices not only provide the isolated logic-to-logic interface function, but due to many unique features of the input amplifier, offer solutions for high speed data communications and precise DC level sensing. These applications, and the operation of the Optologic interface gate, will be discussed in this application note.

OPTOLOGIC OPERATION

Functionally the Optologic gate consists of an input amplifier, high speed GaAsP/GaAs LED emitter, and an output amplifier. Figure 1 illustrates the block diagram of the LSTTL to TTL logic gate.

The input network is a hybrid assembly of a silicon IC amplifier and LED emitter. The input functionally consists of four elements:1) open emitter input with Schottky diode clamp, 2) differential comparator, 3) voltage reference, and 4) current steering LED driver.

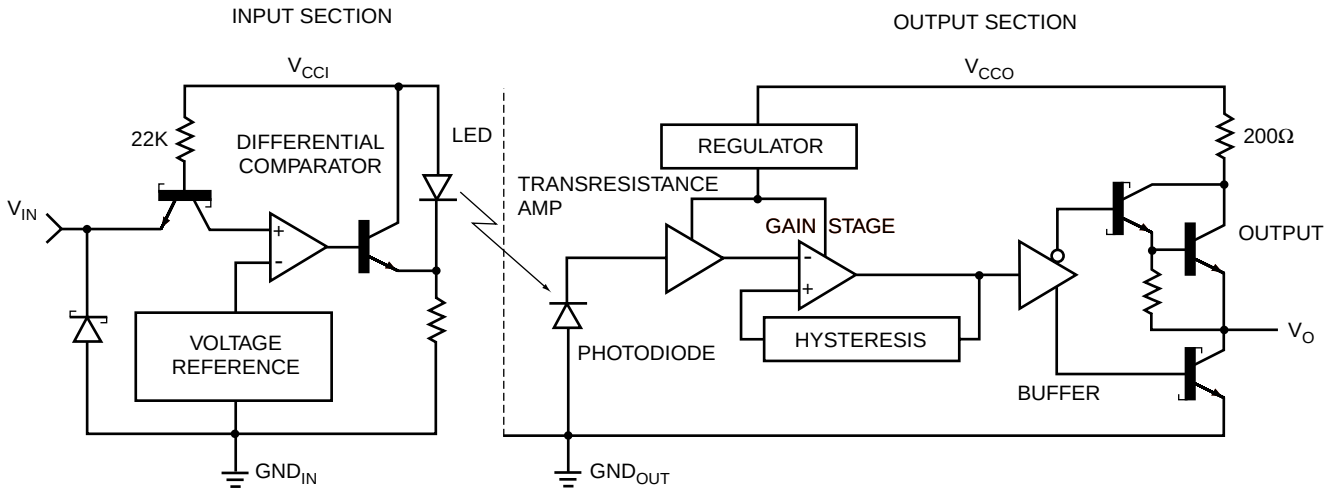


Figure 1. 74OL6000 Block Diagram

The input of the IC is very similar to standard bipolar logic. It consists of a Schottky clamp diode connected between the emitter of an NPN transistor and ground. The input sources input current over the nominal LSTTL logic levels. Figure 2 shows the typical input current/voltage characteristics. The input offers a 20K ohm input resistance between -0.5 and 3.0 V. The input resistance drops to 7.5 K from 3.0 to 3.4 V, while between 3.4 to 7 V the resistance is greater than 1 megohm. Input voltages more negative than -0.5 V activate the Schottky diode clamp.

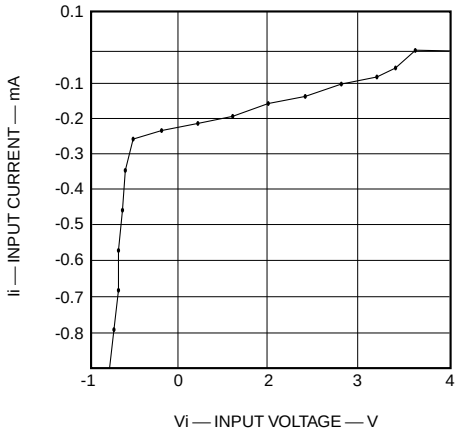


Figure 2. Input Current vs. Input Voltage

The collector of the input transistor is connected to a differential comparator, whose output switches when the input signal exceeds the reference voltage. The effects of temperature and power supply variations are minimized through the use of a voltage reference.

Figure 3 shows V_{IN} vs V_{OUT} of the 74**OL**6000 illustrating the input voltage switching point 1.34 V.

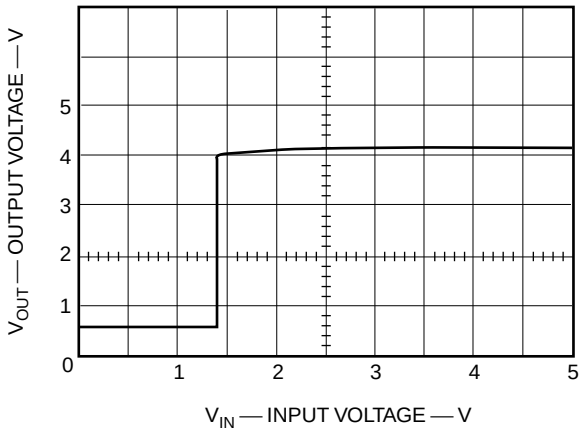


Figure 3. 74OL6000

The output of the comparator controls a current steering LED driver. The LED is enabled when the transistor is OFF. When the transistor is driven into saturation, it steers the current away from the LED by dropping the LED voltage below its 1.5 V conduction threshold. This technique of driving has the advantage of pre-biasing the LED, thus minimizing the switching speed reduction caused by the diode junction capacitance. It has the added advantage of greatly reducing power supply noise.

The output IC consists of seven functional circuits. These include: 1) PN photodiode, 2) transresistance amplifier, 3) differential gain stage, 4) hysteresis loop, 5) buffer amplifier, 6) output stage, and 7) voltage regulator.

The optical flux developed by the LED emitter is converted to an electrical current by a reversed biased PN photodiode. This photocurrent is amplified and converted to a voltage by a transresistance gain stage. This stage is connected to the inverting input of a differential amplifier, while the hysteresis network is connected to the non-inverting input. The output of this amplifier drives a buffer that provides the level shifts and signal splitting needed to drive the totem pole output stage. Power supply noise is rejected through the use of a voltage regulator that powers the transresistance amplifier and the differential gain stage.

The output of the amplifier is offered as either an open collector (74**OL**6010/11) or a totem pole (74**OL**6000/01). The open collector output is designed to interface with CMOS logic, with a supply voltage up to 15 volts. The output transistor will drive 10 standard TTL loads with a V_{OL} of 0.4 V, and its safe operating range allows it to sink up to 60 mA peak. The active pull-up will source an I_{OH} in excess of 10 mA with a V_{OH} greater than 2.4 V. The output characteristics of the Optologic gates are shown in Figures 4 and 5.

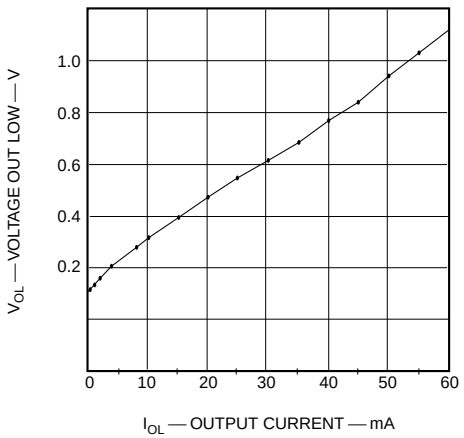


Figure 4. 74OL6000 V_{OL} vs I_{OL}

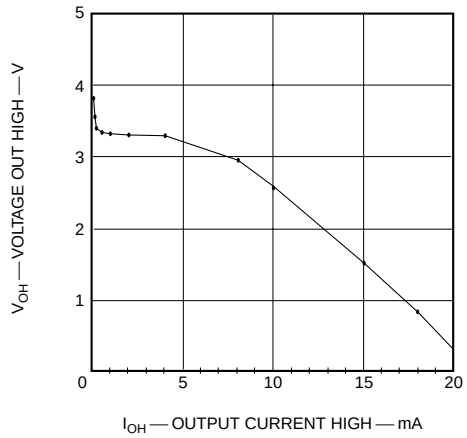


Figure 5. 74OL6000 V_{OH} vs I_{OH}

The effects of common mode transients and other noise sources on the output amplifier are reduced by an optically transparent, electrically conductive noise shield, as well as by amplifier hysteresis. The shield shunts the noise away from the input stage and channels it to logic ground. The amplifier hysteresis eliminates false output pulses caused by a slowly varying input signal, or power supply noise found on the input network of the Optologic gate.

SWITCHING OPERATION

The Optologic optocoupler was designed to interface directly with LSTTL at the input and either TTL or CMOS at the output. In addition, the switching levels are identical to the standards established for each of these logic families.

There are four Optologic devices currently available. Two of these devices are LSTTL to TTL compatible. The 74**OL**6000 is a logic buffer and the 74**OL**6001 is an inverter logic. LSTTL to CMOS is provided by the 74**OL**6010 buffer and the 74**OL**6011 inverter. The switching operation is shown below.

DEVICE	INPUT	LED	OUTPUT
74**OL**6000	HIGH LOW	OFF ON	HIGH LOW
74**OL**6001	HIGH LOW	ON OFF	LOW HIGH
74**OL**6010	HIGH LOW	OFF ON	OFF ON
74**OL**6011	HIGH LOW	ON OFF	ON OFF

The preceding table indicates that the Optologic gate is effectively two cascaded logic gates. the first is the input network and the second the output. Both the totem pole and open collector output amplifier function as inverts. Thus, when the LED is ON, the output will be a logic low state. Therefore, in order to create an Optologic buffer (74**OL**6000, 74**OL**6010), the input amplifier must function as an inverter for controlling the LED emitter. The Optologic inverter gates (74**OL**6001, 74**OL**6011) use a non-inverting input amplifier.

One will note that the output chip is always HIGH (OFF) when the LED is OFF, and the output is forced LOW (ON) when the LED is ON. Thus, the Optologic input has a switching threshold of 1.34 V.

The operational sequence of LED and input/output chips will give the designer insight when combinations of inverters and buffers are used in parallel data transfer applications. In these types of applications, the rate of data transfer is greatly affected by the propagation delay difference between the slowest to fastest Optologic gate. The propagation delay is the sum of the delays of the input chip, LED, and output amplifier. The typical delay times for the 74**OL**6000/01 are 65ns, with rise times of 45ns and fall times of 5ns. The rise and fall time difference is the result of the operation of the output amplifier. The typical switching characteristics of the 74**OL**6000/01 are shown in Figures 6 and 7. When output edge detection is used, the fastest response will be obtained when the falling edge (H-L) is sensed. This is true for both the inverter and buffer Optologic gates.

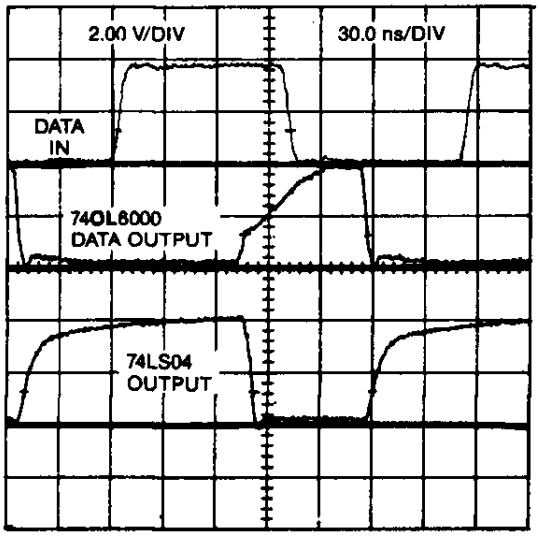


FIGURE 6. 74OL6000 Switching Characteristics

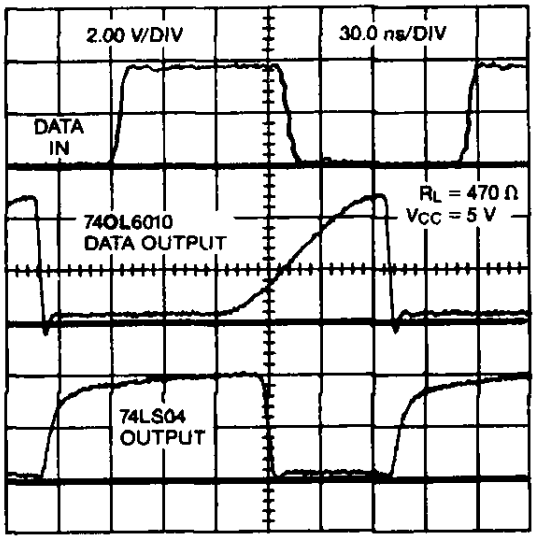


FIGURE 7. 74OL6010 Switching Characteristics

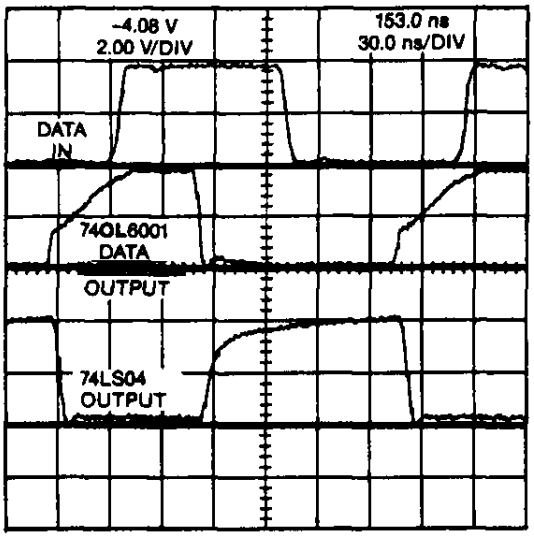


FIGURE 8. 74OL6001 Switching Characteristics

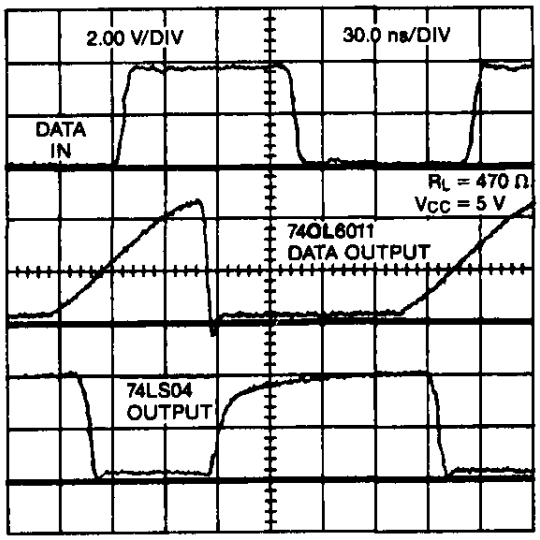


FIGURE 9. 74OL6011 Switching Characteristics

The CMOS compatible output family (74**OL**6010/11) satisfies the V_{OH} by using an open collector transistor and an external pull-up resistor. The high to low propagation delay and fall time is very similar to the 74**OL**6000/01 Optologic gates. The low to high propagation delay and rise time is greatly influenced by the value of the pull-up resistor. When a 470 ohm pull-up resistor is used, the typical propagation delay for low to high is 100ns. The typical switching characteristics of the 74**OL**6010/11 are shown in Figures 8 and 9.

The Optologic gate's input and output chips ensure a constant propagation delay over the temperature range of -40°C to 85°C. This consistency is shown in Figures 10 and 11.

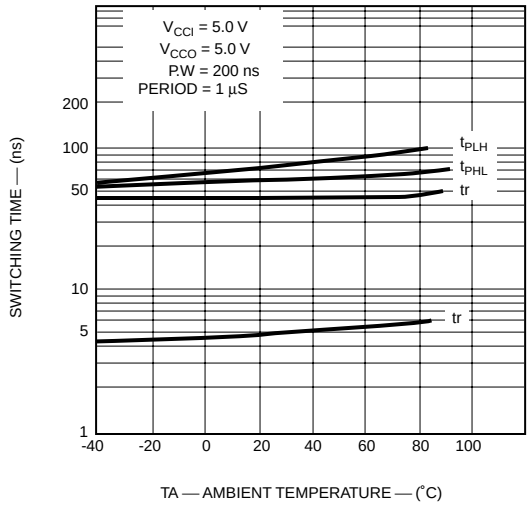


Figure 10. 74OL6000/01 Switching Times vs. Ambient Temperature

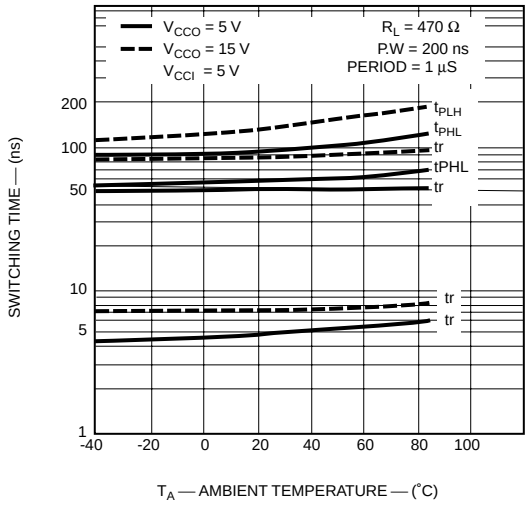


Figure 11. 74OL6010/11 Switching Times vs. Ambient Temperature

OPERATIONAL CONSIDERATIONS

The Optologic gates have eliminated the need to perform a worst case analysis for logic family compatibility and switching speed. Operational performance degradation is greatly minimized through the optimal selection of the LED emitter and output amplifier. These features make the Optologic gates the easiest optocouplers to use for logic-to-logic interfacing.

OPERATIONAL CONSIDERATIONS

The consistent performance of the Optologic gates will be obtained if the designer ensures that package power dissipation and operational supply voltage does not exceed their absolute maximum ratings. The 74**OL**6000/01 were designed to operate from standard 4.5 to 5.5 volt supplies and, under these conditions, the devices will operate successfully over a -40°C to 85°C range. The 74**OL**6010/11 output amplifier will operate from a 15V supply over a temperature range of -40°C to 55°C, however, the output amplifier power supply voltage must be derated at a rate of -0.27V/°C above an operational temperature of 55°C. This function is shown graphically in Figure 12.

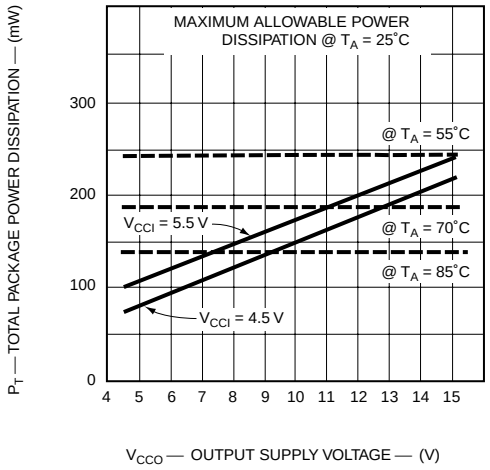


Figure 12. Power Dissipation vs. Ambient Temperature

Operational stability is optimized when low impedance V_{CC} and V_{DD} supplies are used to power the Optologic gates. This can be ensured by the common practice of including 0.1 µF bypass capacitors for the input and output amplifier supplies. These capacitors are placed immediately next to the V_{CC} and ground connections of the input and output amplifier. These capacitors minimize output ringing and improve the power supply noise rejection. A suggested printed circuit board layout is shown in Figure 13.

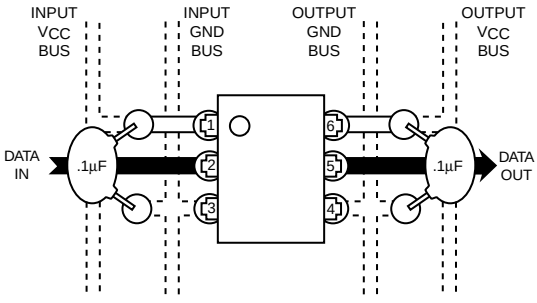


Figure 13. Suggested PCB Lay-Out

DATA COMMUNICATIONS INTERFACING

The common LED input/phototransistor output and high speed logic compatible output have found their way into point-to point (simplex) data communications applications. When used as a line receiver the designer was required to design a matching network to provide the minimum reflection caused by the non-linear input impedance of the light emitting diode. These matching networks were commonly designed for a specific cable distance between the receiver and the transmitter. Therefore, if the cable distance were to be changed, a new matching network would be required in order to effect proper operation.

This need of designing matching networks and allowing only point-to-point communications is a thing of the past with the introduction of the Optologic gates. The Optologic gate, when used as a line receiver, does not require a matching network. Its input amplifier offers a 22Kohm input resistance which permits it to bridge the transmission. When it is used as the only receiver connected to the end of the transmission line, optimum speed performance will be obtained when the transmission line is terminated in its characteristic impedance (Zo).

When multiple data taps are required, all the designer needs to do is bridge the Optologic gate across the transmission line at the desired cable length. Figure 14 illustrates a simplex multi-drop (tap) data communications system that has incorporated four 74**OL**6001 gates as receivers, evenly spaced along 1000 foot, 75 ohms co-axial transmission line. The cable used in this example is a Times Fiber & Cable Model RG59/U Series 2000. This cable includes a third insulated conductor that is used as the V_{CC} supply source for the input amplifier of the Optologic gates connected to the transmission line. This third conductor permits one simple isolated supply to power all the Optologic gates connected to the communications cable.

The common mode rejection and insulation of the communications system can be greatly improved by incorporating an Optologic gate as a line driver. When driving low impedance transmission lines such as the 75 ohm coax shown in Figure 14, a buffer is required to drive the line. This buffer is shown in Figure 15.

The signal quality “Eye Pattern” for the communications system shown in Figure 14 is provided in Figures 16 through 18 with a 10 MBaud NRZ Pesudo-Random Sequence (PRS). Traces 1-3 in Figure 16 describe the transmitter section. Traces 4-7 of Figure 17 show the output of the four Optologic bridged terminations. Traces 8-11 in Figure 18 illustrate the “Eye Pattern,” as seen at the output of the 74**LS**04 logic gate. the data quality is well reserved, in that only a 30% eye closure is seen at the receiver located 1000 feet from the transmitter.

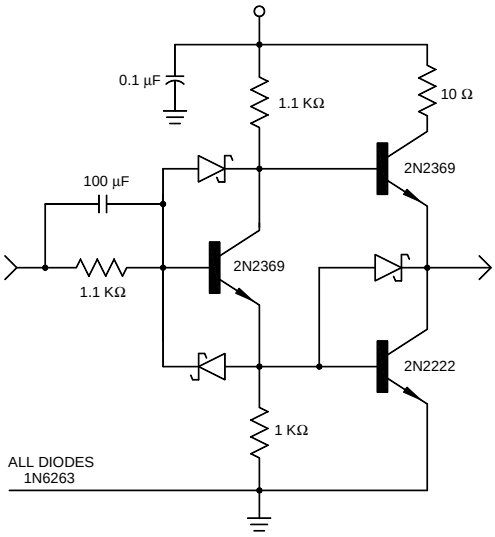


Figure 15. Buffer

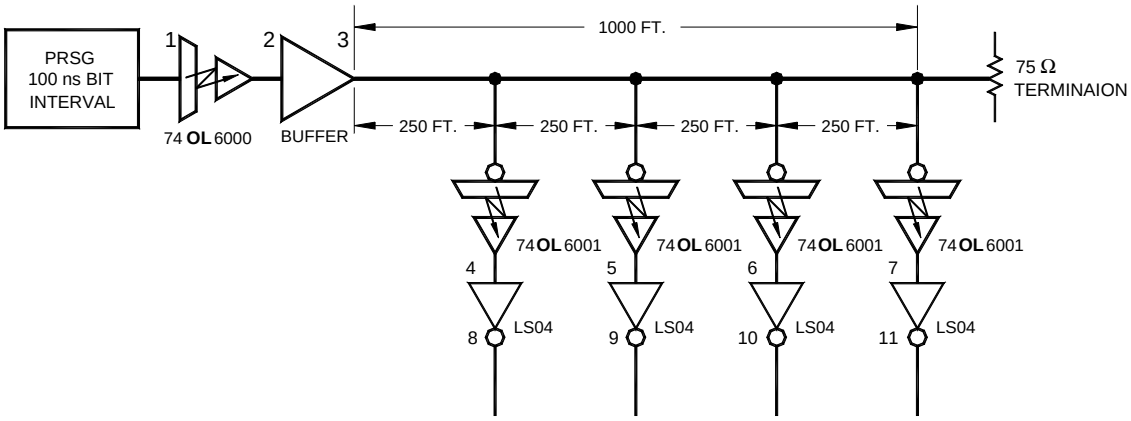
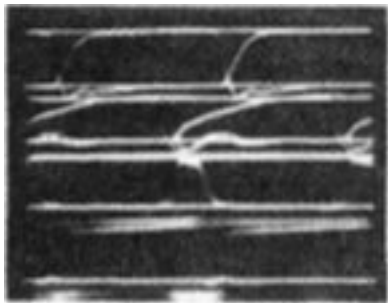
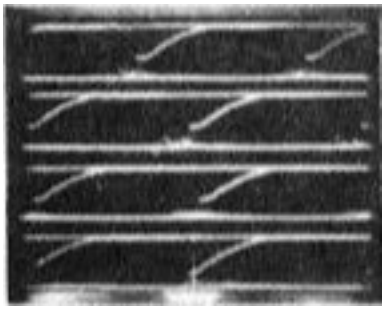


Figure 14. Simplex Multi-Drop Data Communicatins System



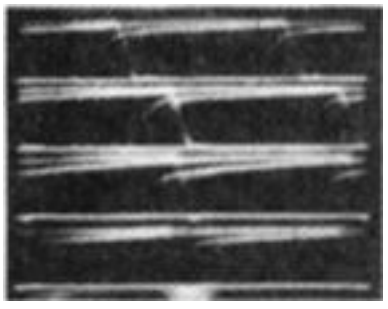
HORIZONTAL = 20 ns/DIV
VERTICAL = 2 V/DIV

Figure 16



HORIZONTAL = 20 ns/DIV
VERTICAL = 2 V/DIV

Figure 17



HORIZONTAL = 20 ns/DIV
VERTICAL = 2 V/DIV

Figure 18

Through the use of the tri-state line driver, shown in Figure 19, a half duplex multi-drop communications system can be configured. This is done by adding this driver at each of the tap positions shown in Figure 14. This system provides the most common data communications configuration of the high speed bi-directional communications, with the added features of vastly improved common mode transient rejection and insulation when compared to a common integrated line receiver.

When high differential and common mode rejection are required, the differentially driven and received communications topology is considered. Figure 29 shows a full duplex point-to-point communications system that is implemented with twisted pair shielded cable. Given the higher impedance of this type of cable, it is possible for the Optologic gates to drive the line directly. Here, a 74**OL**6000 and 74**OL**6001 are used in a push-pull mode to differentially drive the line. the receiving end of the line is simply terminated in Zo. Bridging this termination is a DM8820 differential line receiver that is connected to the 74**OL**6000 Optologic gate. Power for the line receiver and the Optologic gate is derived from two insulated shields of the twisted pair cable. This system offers a data rate is excess of 1 Mbaud NRZ at a distance of 600 feet.

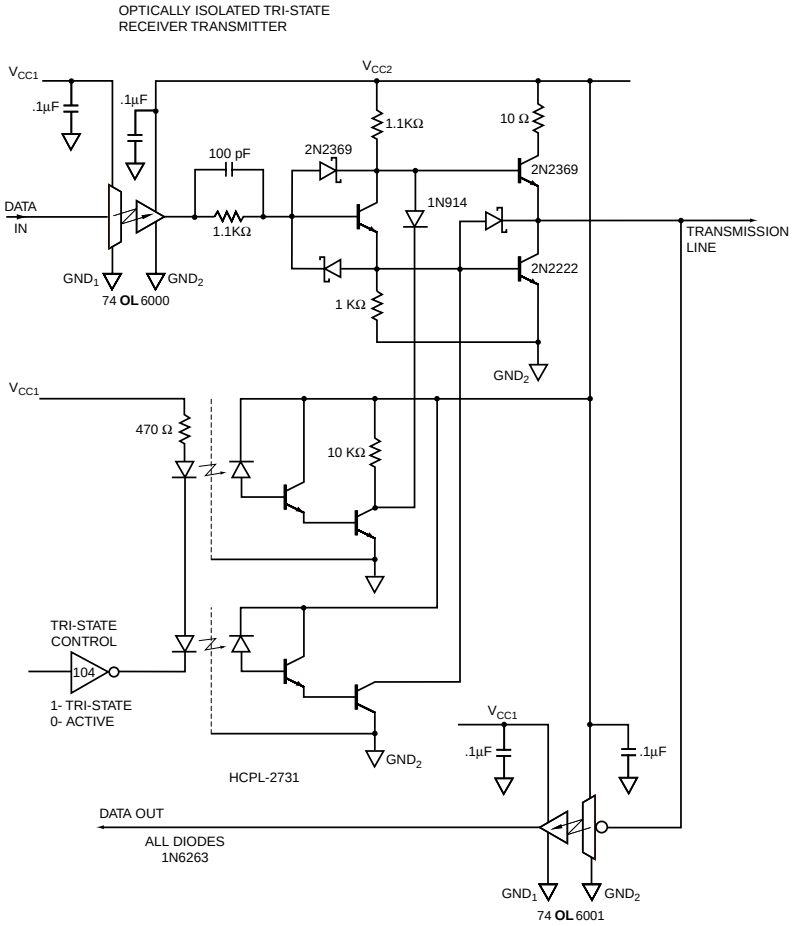


Figure 19

AC VOLTAGE LEVEL MONITOR

The machine and process control industry has used optocouplers as voltage sensing devices for a number of years. These have proven very versatile when the presence or absence of power is to be determined. the monitoring of specific voltage levels has required the designer to commonly use selected couplers that have guaranteed gain at a specific LED drive current. Once armed with this specification, a resistor divider network is designed that will support 1 to 10 mA required by the LED. As the line voltage threshold increases, the power dissipation in the passive divider network can approach 2 watts.

Using the Optologic gate, a fixed AC or DC level monitor can easily be designed. Recall the Optologic gate has a fixed reference source built into the input amplifier. The stability and consistency of this reference source allows the designer to construct a level detector using standard product that will offer an accuracy of ±15%. If higher accuracy is needed, the factory can provide devices with tighter reference voltage tolerance. Not only is high accuracy possible, but power required from the line is typically less than 0.2W.

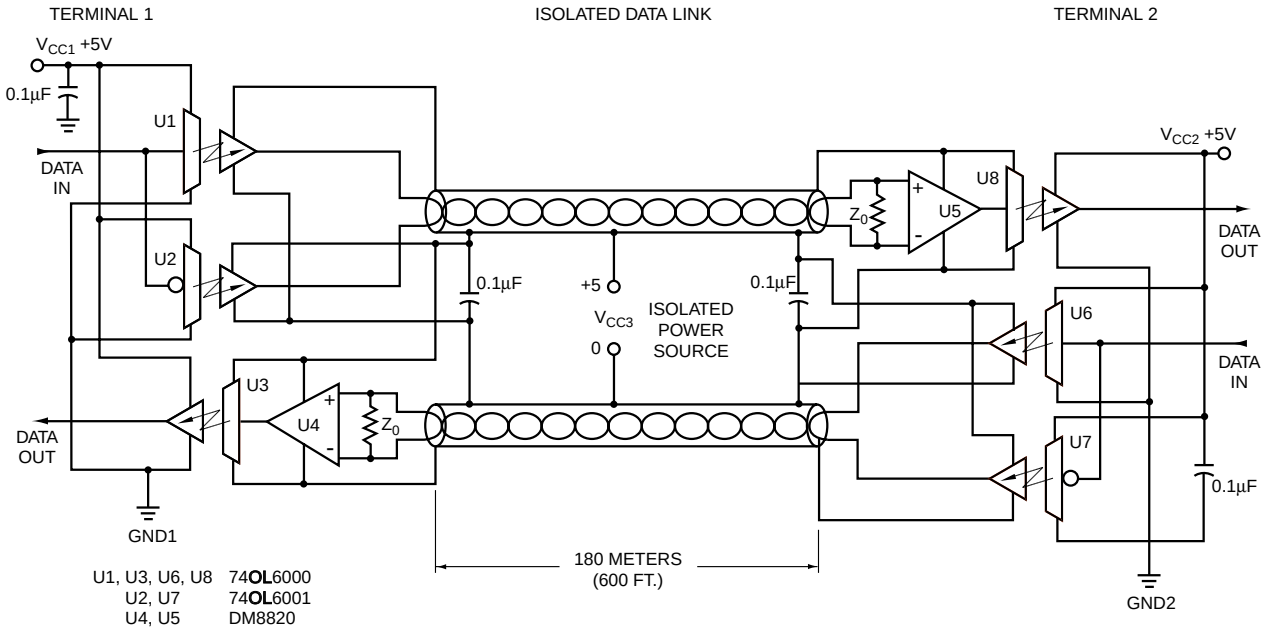


Figure 20. 1 MBaud Full Duplex Differential Optically Isolated Transmit and Receive Data Transmission System with Shielded Twisted Pair.

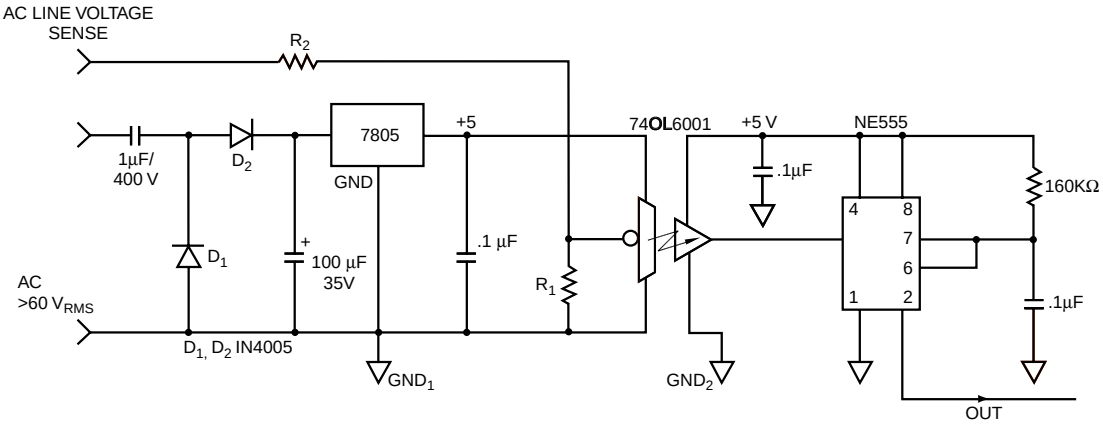


Figure 21. Optologic Voltage Line Monitor and Power Supply

The most significant feature of the Optologic, in this application, is the small amount of current that is required to flow in the voltage divider. Under worst case design considerations, this sensing current will not exceed 500 µA. This low current permits the use of .25 W or smaller precision resistors, thus allowing even greater monitor accuracy.

For example, when sensing a voltage of 110 VAC, the power dissipated in the divider network is only 45mW.

Figure 32 shows a typical AC Line Monitor circuit. The threshold is determined by selecting the value of R1 and R2. Best accuracy is achieved when R1 is equal to or less than 2.2Kohm. Once R1 is selected, the value of R2 can be determined with the following equation.

$$R2 = \frac{R1\ R_N\ (Vth - Vref)}{Vref(R_N + R1) - R1V}$$

Where

Vth = Selected AC or DC switching level
Vref = 1.34V
R_N = 22KΩ
V = 4.3V

This equation has been solved graphically in Figure 22.

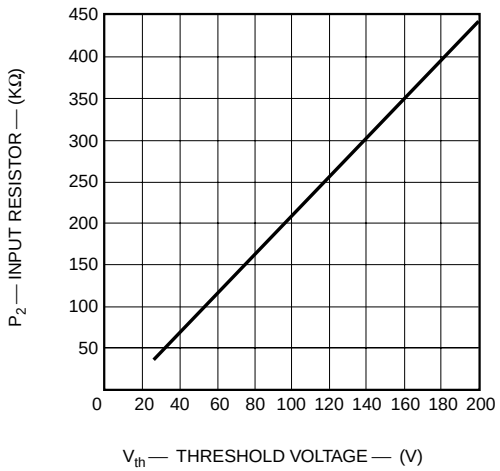


Figure 22. Input Resistor vs. Threshold Voltage

The monitor circuit shown in Figure 21 consists of three elements. The first is an Optologic power supply, the second is the voltage divider, and the third is the retriggerable one-shot.

The power supply consists of the capacitor voltage divider and 5V regulator. A capacitor divider was used to minimize the power consumption from the AC line. This power supply will provide over 15 mA when the line voltage exceeds 60V RMS.

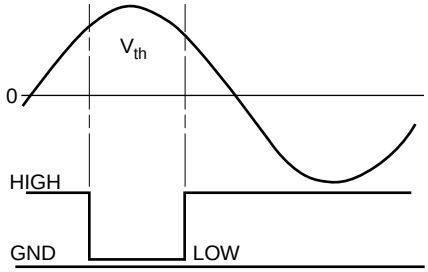


Figure 23. 74OL0001 AC Level Detection Waveform

The voltage divider (R1, R2) sets the monitor threshold point of the sensor. R1 is used as an Optologic input pull-down, thus, as the input voltage rises, it forces current through R1 which raises its voltage up to the Vref of the Optologic input. Once the reference voltage is exceeded, the output of the Optologic will change state. Figure 23 illustrates the relationship of the input voltage to the 74**OL**6001 output. It can be seen that the output is a series of pulses, whose width is determined by the duration that the input waveform exceeds the voltage threshold.

The final section of the sensor consists of a retriggerable one-shot, constructed with an NE555 timer. This one-shot is included to convert the pulse train into a constant logic level. For best stability, a time constant of 1-1/4 cycles was selected. When a 60Hz power main is to be monitored, this becomes a time constant of 18ms. Thus, as the input voltage exceeds the monitor threshold, the output of the 74**OL**6001 changes from high to low, thus triggering the NE555 timer. Once triggered, the NE555 outputs a logic high and will stay high as long as it is triggered every 16ms.

CONCLUSION

The Optologic family of TTL and CMOS compatible devices is a new and easy-to-use optically coupled logic circuit element. This Application Note has provided but few of many new uses for this versatile device. Not only does this device provide high noise immunity and level shifting for logic-to-logic interfaces, it also has numerous applications in data communications and industrial control systems.

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