NT7502

Preliminary

65 × 132 RAM-Map LCD Controller/Driver

Features

- Direct RAM data display using the display RAM. When RAM data bit is 0, it is not displayed. When RAM data bit is 1, it is displayed. (At normal display)
- RAM capacity: 65 × 132 = 8580 bits
- Many command functions: Read/Write Display Data. Display ON/OFF. Normal/Reverse Display. Page Address Set. Set Display Start Line. Set LCD Bias, Electronic contrast Controls, V0 voltage regulation internal resistor ratio set, Read Modify Write, Select Segment Driver Direction, Power Save
- High-speed 8-bit microprocessor interface allowing direct connection to both the 8080 and 6800.
- Serial interface
- Power supply voltage: 2.4 - 3.5V
- Maximum 12V LCD driving output voltage
- 2X / 3X / 4X on chip DC-DC converter
- Voltage regulator
- Voltage follower
- On chip oscillator

General Description

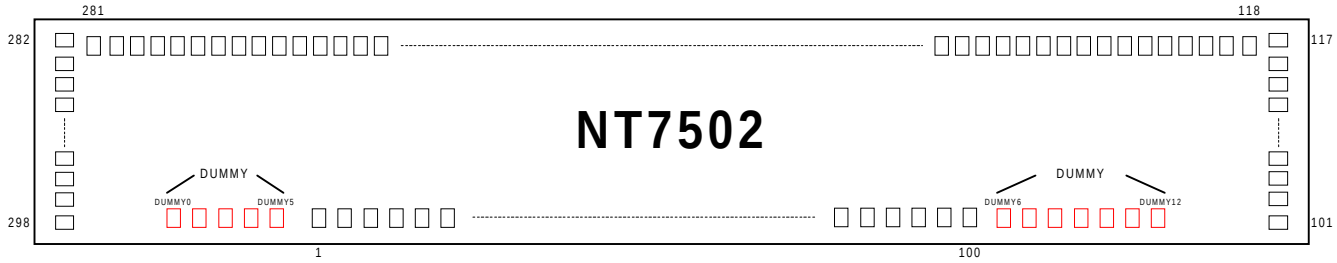
The NT7502 is a single-chip LCD driver for dot-matrix liquid crystal displays, which is directly connectable to a microcomputer bus. It accepts 8-bit serial or parallel display data directly sent from a microcomputer and stores it in an on-chip display RAM. It generates a LCD drive signal independent of microprocessor clock.

The set of the on-chip display RAM of 65 × 132 bits and a one-to-one correspondence between LCD panel pixel dots and on-chip RAM bits permits implementation of displays with a high degree of freedom.

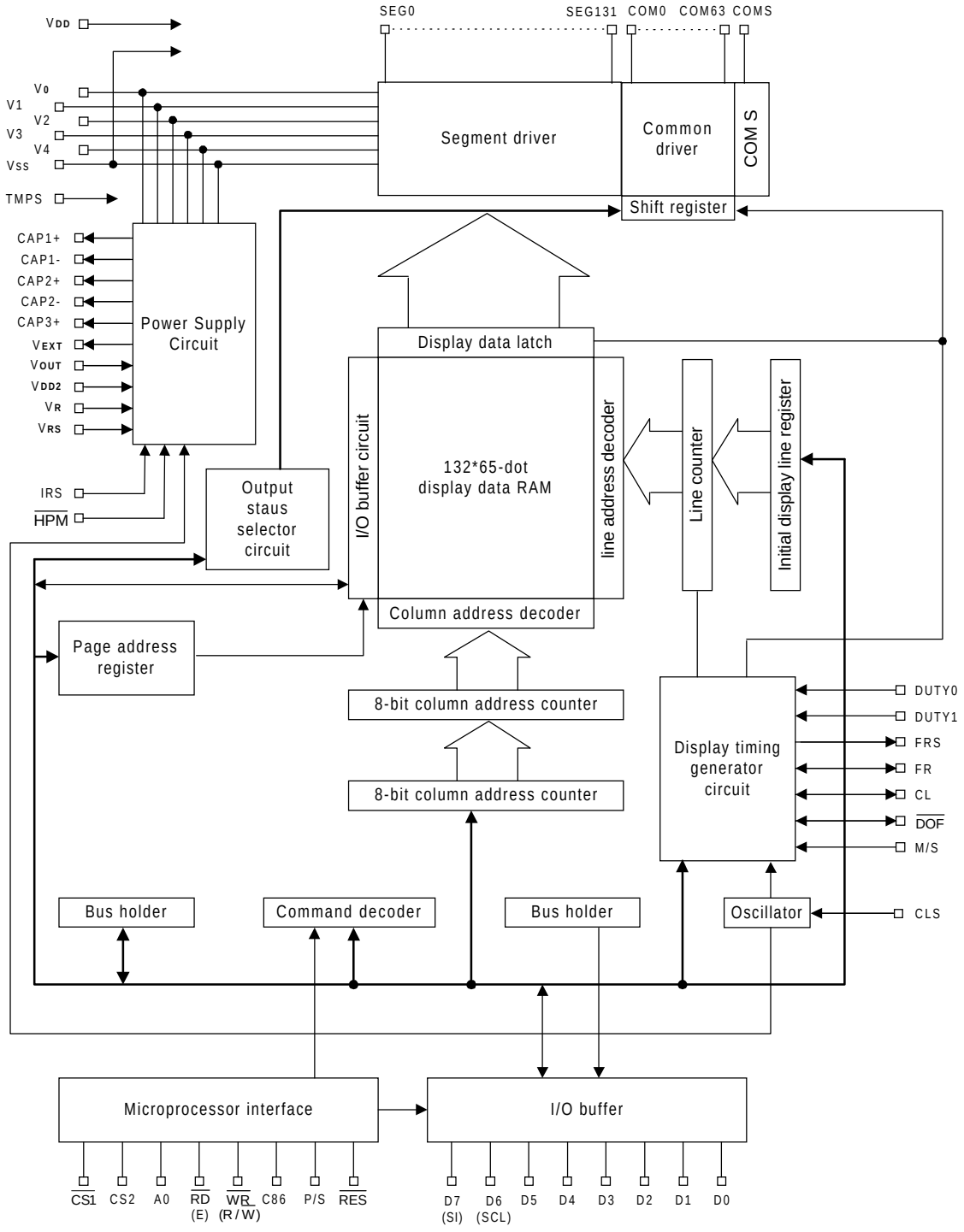
The NT7502 contain 65 common output circuits and 132 segment output circuits, so that a single chip of NT7502 can make 65 x 132, 55 x132, 49x132 and 33 x 132 dots displays with pad option (DUTY1, DUTY0).

No external operation clock is required for RAM read/write operations. Accordingly, this driver can be operated with a minimum current consumption and its on-board low-current-consumption liquid crystal power supply can implement a high-performance handy display system with a minimum current consumption and a smallest LSI configuration.

Pad Configuration



Block Diagram



Pad Description

Power Supply

Pad No.	Symbol	I/O	Description
10, 16, 26, 30-33, 53, 71, 77, 81, 91	V_{DD}	Supply	2.4 - 3.5V power supply. Connect to microprocessor power supply pin Vcc
34-36	V_{DD2}	Supply	This is the reference power supply for the step-up voltage circuit for the LCD
7, 13, 25, 29, 37-40, 56, 69-70, 74, 79, 83, 89	V_{SS}	Supply	Ground
65-66 V_0 57-58 V_1 59-60 V_2 61-62 V_3 63-64 V_4		Supply	LCD driver supply voltages. The voltage determined by LCD cell is impedance-converted by a resistive driver or an operation amplifier for application. Voltages should be the following relationship: $V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$ When the on-chip operating power circuit is on, the following voltages are given to V_1 to V_4 by the on-chip power circuit. Voltage selection is performed by the Set LCD Bias command.

LCD bias	V1	V2	V3	V4
1/5 bias	4/5V0	3/5V0	2/5V0	1/5V0
1/6 bias	5/6V0	4/6V0	2/6V0	1/6V0
1/7 bias	6/7V0	5/7V0	2/7V0	1/7V0
1/8 bias	7/8V0	6/8V1	2/8V0	1/8V0
1/9 bias	8/9V0	7/9V0	2/9V0	1/9V0

LCD Driver Supplies

Pad No.	Symbol	I/O	Description
45-46	CAP1-	O	Capacitor 1- pad for internal DC/DC voltage converter
47-48	CAP1+	O	Capacitor 1+ pad for internal DC/DC voltage converter
51-52	CAP2-	O	Capacitor 2- pad for internal DC/DC voltage converter
49-50	CAP2+	O	Capacitor 2+ pad for internal DC/DC voltage converter
43-44	CAP3+	O	Capacitor 3+ pad for internal DC/DC voltage converter
41-42	V_{OUT}	O	DC/DC voltage converter output
67-68	V_R	I	Voltage adjustment pad. Applies voltage between V_0 and V_{SS} using a resistive divider.
54	V_{EXT}	I	This is the external input reference voltage (V_{REF}) for the internal voltage regulator. It is valid only when external VREF is used. V_{EXT} must be ≥ 2.4V and ≤ V_{DD2} When using internal V_{REF}, this pad must be NC
82	TMPS	I	Selects temperature coefficient of the reference voltage TMPS = 0: -0.05% / °C TMPS = 1: -0.2 % / °C
55	VRS	I	Select the internal voltage regulator or external voltage regulator, VRS = 0: using the external V_{REF} VRS = 1: using the internal V_{REF}

System Bus Connection Pads

Pad No.	Symbol	I/O	Description
17-24	D0 – D7 (SI) (SCL)	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S="L"), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance. When the chip select is inactive, D0 to D7 are set to high impedance.
12	A0	I	This is connected to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0="H": Indicate that D0 to D7 are display data. A0="L": Indicates that D0 to D7 are control data.
11	$\overline{RES}$	I	When $\overline{RES}$ is set to "L", the settings are initialized. The reset operation is performed by the $\overline{RES}$ signal level.
8, 9	$\overline{CS1}$ CS2	I	This is the chip select signal. When $\overline{CS1}$="L" and CS2="H", then the chip select becomes active,and data/command I/O is enabled
15	$\overline{RD}$ (E)	I	When connected to an 8080 MPU, it is active LOW. This pad is connected to the $\overline{RD}$ signal of the 8080MPU, and the NT7502 data bus is in an output status when this signal is "L". When connected to a 6800 Series MPU , this is active HIGH. This is used as an enable clock input of the 6800 series MPU.
14	$\overline{WR}$ (R/$\overline{W}$)	I	When connected to an 8080 MPU, this is active LOW. This terminal connects to the 8080 MPU $\overline{WR}$ signal . The signals on the data bus are latched at the rising edge of the $\overline{WR}$ signal. When connected to a 6800 Series MPU: This is the read/write control signal input terminal. When R/$\overline{W}$ ="H": Read. When R/$\overline{W}$ ="L": Write.
75	C86	I	This is the MPU interface switch terminal. C86="H": 6800 Series MPU interface. C86="L": 8080 MPU interface.
76	P/S	I	This is the parallel data input/serial data input switch terminal. P/S="H": Parallel data input. P/S="L": Serial data input. The following applies depending on the P/S status: P/S: "H" — Data/Command: A0 — Data: D0 to D7 — Read/Write: $\overline{RD}$ $\overline{WR}$ — Serial Clock: — P/S: "L" — Data/Command: A0 — Data: SI (D7) — Read/Write: Write only — Serial Clock: SCL (D6) When P/S="L", D0 to D5 are HZ. D0 to D5 may be "H", "L" or Open. $\overline{RD}$ (E) and $\overline{WR}$ (P/$\overline{W}$) are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported.
73	CLS	I	Terminal to select whether enable or disable the display clock internal oscillator circuit. CLS="H": Internal oscillator circuit is enabled CLS="L": Internal oscillator circuit is disabled (requires external input) When CLS="L", input the display clock through the CL pad

System Bus Connection Pads (continue)

Pad No.	Symbol	I/O	Description
72	M/S	I	This terminal selects the master/slave operation for the NT7502 chips. Master operation outputs the timing signals that are required for the LCD display, while slave operation inputs the timing signals require for the liquid crystal display, synchronizing the liquid crystal display system.
4	CL	I/O	This is the display clock input terminal. When the NT7502 chips are used in master/slave mode, the various CL terminals must be connected
3	FR	I/O	This is the liquid crystal alternating current signal I/O terminal. M/S="H": Output M/S="L": Input When the NT7502 chip is used in master/slave mode, the various FR terminals must be connected.
5	$\overline{DOF}$	I/O	This is the liquid crystal display blanking control terminal. M/S="H": Output M/S="L": Input When the NT7502 chip is used in master/slave mode, the various $\overline{DOF}$ terminals must be connected
2	FRS	O	This is the output terminal for the static drive. This terminal is only enabled when the static indicator display is ON when in master operation mode, and is used in conjunction with the FR terminal.
80	IRS	I	This terminal selects the resistors for the V0 voltage level adjustment. IRS="H", Use the internal resistors IRS="L", Do not use the internal resistors. The V0 voltage level is regulated by an external resistive voltage divider attached to the VR terminal. This pad is enabled only when the master operation mode is selected. It is fixed to either "H" or "L" when the slave operation mode is selected.
78	$\overline{HPM}$	I	This is the power control terminal for the power supply circuit for liquid crystal drive. $\overline{HPM}$ ="H", Normal mode $\overline{HPM}$ ="L", High power mode This pad is enabled only when the master operation mode is selected. It is fixed to either "H" or "L" when the slave operation mode is selected.

Liquid Crystal Drive Pads

Pad No.	Symbol	I/O	Description
134-265	SEG0 - 131	O	Segment signal output for LCD display
101-132 266-297	COM31 - 0 COM32 - 63	O	Common signal output for LCD display . When in master/slave mode, the same signal is output by both master and slave
133, 298	COMS	O	These are the COM output terminals for the indicator. Both terminals output the same signal. No connect these terminals if they are not used. When in master/slave mode, the same signal is output by both master and slave.

Configuration Pads

Pad No.	Symbol	I/O	Description
27, 28	DUTY0, DUTY1	I	Select the LCD driver duty DUTY1 / DUTY0 / LCD driver duty 0 / 0 / 1/33 0 / 1 / 1/49 1 / 0 / 1/55 1 / 1 / 1/65

Test Pads

Pad No.	Symbol	I/O	Description
84, 86, 88	TEST0 - 2	I	Test pads, no connection for user.
90	TEST3	I	Test pads, and must be connect to V_{DD} or V_{SS}.

Functional Description

Microprocessor Interface

Interface type selection

The NT7502 can transfer data via 8-bit bi-directional data bus (D7 to D0) or via serial data input (SI). When high or low is selected for the parity of P/S pad, either 8-bit parallel data input or serial data input can be selected as shown in Table 1. When serial data input is selected, the RAM data cannot be read out.

Table 1

P/S	Type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D0 to D5
H	Parallel Input	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D0 to D5
L	Serial Input	$\overline{CS1}$	CS2	A0	-	-	-	SI	SCL	(HZ)

"-" Must always be high or low

Parallel Input

When the NT7502 selects parallel input (P/S = high), the 8080 series microprocessor or 6800 series microprocessor can be selected by causing the c86 pad to go high or low as shown in Table 2.

Table 2

C86	Type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	WR	D0 to D7
H	6800 microprocessor bus	$\overline{CS1}$	CS2	A0	E	$R/\overline{W}$	D0 to D7
L	8080 microprocessor bus	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7

Data Bus Signals

The NT7502 identifies the data bus signal according to A0, E, $R/\overline{W}$ ($\overline{RD}$, $\overline{WR}$) signals.

Table 3

Common	6800 processor	8080 processor		Function
A0	($R/\overline{W}$)	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads display data.
1	0	1	0	Writes display data.
0	1	0	1	Reads status.
0	0	1	0	Writes control data in internal register. (Command)

Serial Interface (P/S is low)

When the serial interface has been selected(P/S="L") then when the chip is in active state ($\overline{CS1}$="L" and CS2="H") the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of eighth serial clock for the processing.

The A0 input is used to determine whether or the serial data input is display data, and when A0="L" then the data is command data. The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active.

Figure 1 is serial interface signal chart.

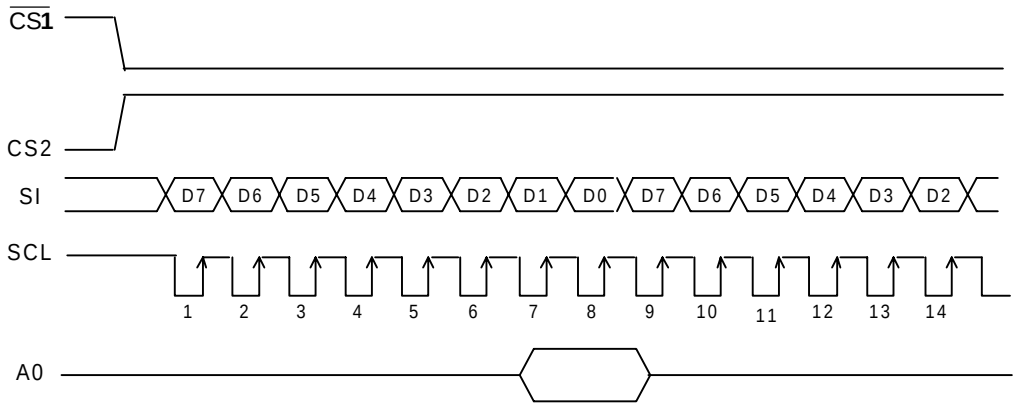


Figure 1

- When the chip is not active, the shift registers and the counter are reset to their initial states.
- Reading is not possible while in serial interface mode.
- Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

Chip Select Inputs

The NT7502 has two chip select pads. $\overline{CS1}$ and CS2 and can interface to a microprocessor when $\overline{CS1}$ is low and CS2 is high.

When these pads are set to any other combination. D0 to D7 are high impedance and A0, E and $R/\overline{W}$ inputs are disabled. When serial input interface is selected. the shift register and counter are reset.

Access to Display Data RAM and Internal Registers

The NT7502 can perform a series of pipeline processing between LSI's using bus holder of internal data bus in order to match the operating frequency of display RAM and internal registers with the microprocessor. For example, the microprocessor reads data from display RAM in the first read (dummy) cycle, stores it in bus holder, and outputs it onto system bus in the next data read cycle.
Also, the microprocessor temporarily stores display data in bus holder, and stores it in display RAM until the next data write cycle starts.
When viewed from the microprocessor, the NT7502 access speed greatly depends on the cycle time rather than access time to the display RAM (t_{ACC}). It shows the data transfer speed to/from the microprocessor can increase. If the cycle time is inappropriate, the microprocessor can insert the NOP instruction that is equivalent to the wait cycle setup. However, there is a restriction in the display RAM read sequence. When an address is set, the specified address data is NOT output at the immediately following read instruction. The address data is output during second data read. A single dummy read must be inserted after address setup and after write cycle (refer to Figure2).

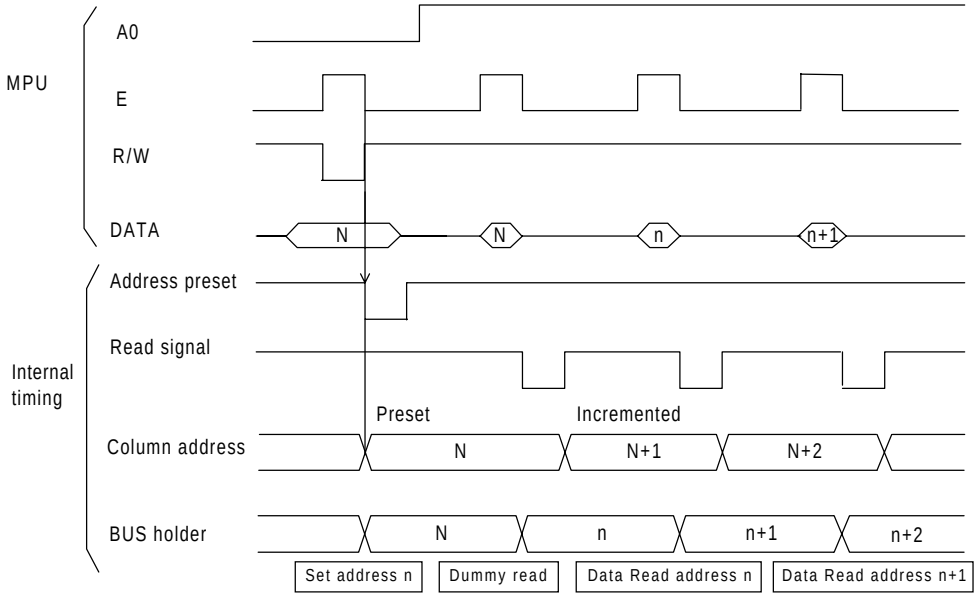


Figure 2

Busy Flag

When the busy flag is "1" it indicates that the NT7502 chip is running internal processes, and at this time no command aside from a status read will be received. The busy flag is outputted to D7 pad with the read instruction. If the cycle time (t**CYC**) is maintained, it is not necessary to check for this flag before each command. This makes vast improvements in MPU processing capabilities possible.

Display Data RAM

Display Data RAM
The display data RAM is a RAM that stores the dot data for the display. It has a 65(8 page * 8 bit+1)*132 bit structure. It is possible to access the desired bit by specifying the page address and the column address. Because, as is shown in Figure3, the D7 to D0 display data from the MPU corresponds to the liquid crystal display common direction, there are few constraints at the time of display common direction, there are few constraints at the time of display data transfer when multiple NT7502 chips are used, thus and display structures can be created easily and with a high degree of freedom.
Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, it will not cause adverse effects on the display (such as flickering).

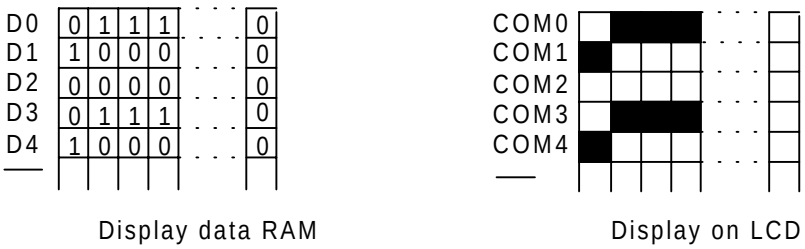


Figure 3

The Page Address Circuit

As shown in Figure 4, page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access.
Page address8 (D3, D2, D1, D0=1, 0, 0, 0,) is the page for the RAM region used only display data D0 is used.

The Column Address

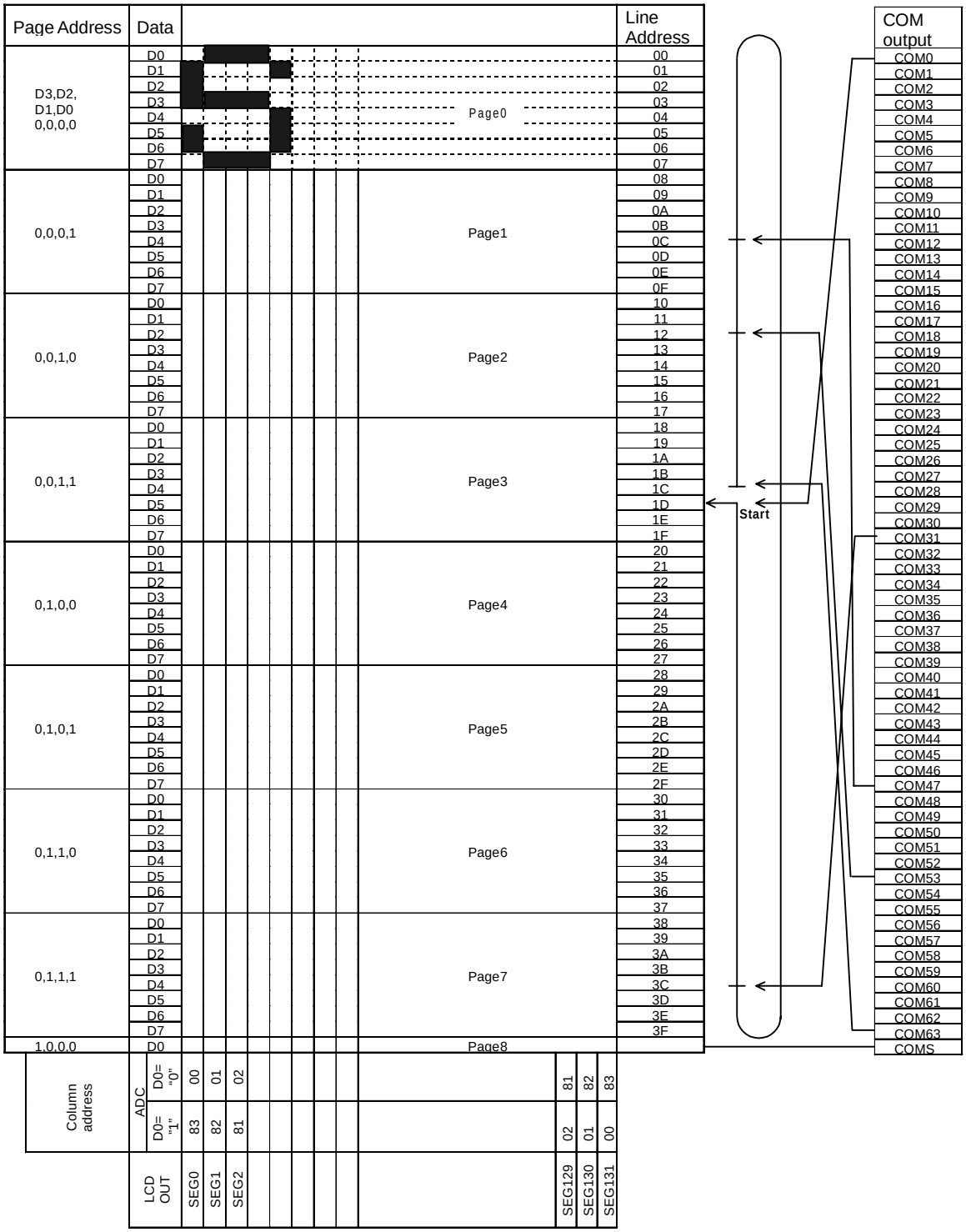
As is shown in Figure 4, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/ write command. This allows the MPU display data to be accessed continuously. Moreover, the incrimination of column addresses stops with 83H. because the column address is independent of the page address, when moving, for example, from page0 column 83H to page 1 column 00H, it is necessary to respecify both the page address and the column address.
Furthermore, as is shown in Table 4, the ADC command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the LCD module is assembled can be minimized.

Table 4

SEG Output	SEG0		SEG131
ADC"0"	0(H)→	Column Address	→83(H)
(ADC)"1"	83(H)←	Column Address	←0(H)

The Line Address Circuit

The line address circuit, as shown in Table 4, specifies the line address relating to the COM output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified (this is the COM0 output when the common output mode is normal, and the COM63 output for NT7502, when the common output mode is reversed. The display area is a 65 line area for the NT7502 from the display start line address.
If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. can be performed Relationship between display data RAM and address (if initial display line is 21H)


Page Address
Data
Line Address
COM output
D3,D2, D1,D0 0,0,0,0
Page0
0,0,0,1
Page1
0,0,1,0
Page2
0,0,1,1
Page3
0,1,0,0
Page4
0,1,0,1
Page5
0,1,1,0
Page6
0,1,1,1
Page7
1,0,0,0
Page8
Start
COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10
COM11
COM12
COM13
COM14
COM15
COM16
COM17
COM18
COM19
COM20
COM21
COM22
COM23
COM24
COM25
COM26
COM27
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COM38
COM39
COM40
COM41
COM42
COM43
COM44
COM45
COM46
COM47
COM48
COM49
COM50
COM51
COM52
COM53
COM54
COM55
COM56
COM57
COM58
COM59
COM60
COM61
COM62
COM63
COMS
Column address
ADC
D0= "0"
D0= "1"
LCD OUT
00 01 02 ... 81 82 83
83 82 81 ... 02 01 00
SEG0 SEG1 SEG2 ... SEG129 SEG130 SEG131

Figure 4

The Display Data Latch Circuit

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM.
Because the display normal/reverse status, display ON/OFF status, and display all points ON/OFF commands control only the data within the latch, they do not change the data within the display data RAM itself.

The Oscillator Circuit

This is a CR-type oscillator that produces the display clock. The oscillator circuit is only enabled when M/S="H' and CLS="H". When CLS= "L" the oscillation stops, and the display clock is input through the CL terminal.

Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of accesses to the display data RAM by the MPU. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, there is absolutely no adverse effect (such as flickering) on the display.
Moreover, the display timing generator circuit generates the common timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a drive wave form using a 2 frame alternating current drive method, as is shown in Figure 5, for the liquid crystal drive circuit.
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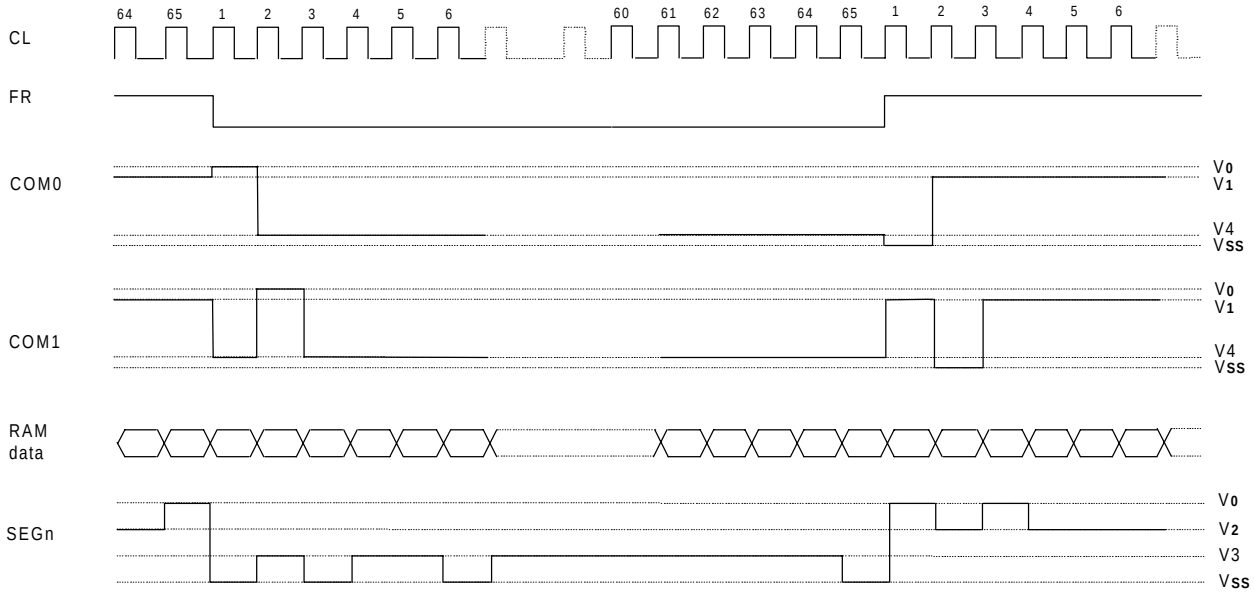


Figure 5

When multiple NT7502 chips are used, the slave chips must be supplied the display timing signals (FR, CL, $\overline{DOF}$) from the master chip[s].

Table 5 shows the status of the FR, CL, and $\overline{DOF}$ signals.

Table 5

Operating Mode		FR	CL	$\overline{DOF}$
Master (M/S="H")	The internal oscillator circuit is enabled (CLS="H")	Output	Output	Output
	The internal oscillator circuit is disabled (CLS="L")	Output	Input	Output
Slave (M/S="L")	The internal oscillator circuit is disabled (CLS="H")	Input	Input	Input
	The internal oscillator circuit is disabled (CLS="L")	Input	Input	Input

Table 6 shows the relationship between oscillation frequency and frame frequency

Table 6

Duty	Item	f_{CL}	f_{FR}
1/65	On-chip oscillator is used	fosc/6	$f_{CL}/(2\times65)$
	On-chip oscillator is not used	External input f_{CL}	$f_{CL}/(2\times65)$
1/55	On-chip oscillator is used	fosc/8	$f_{CL}/(2\times55)$
	On-chip oscillator is not used	External input f_{CL}	$f_{CL}/(2\times55)$
1/49	On-chip oscillator is used	fosc/8	$f_{CL}/(2\times49)$
	On-chip oscillator is not used	External input f_{CL}	$f_{CL}/(2\times49)$
1/33	On-chip oscillator is used	fosc/12	$f_{CL}/(2\times33)$
	On-chip oscillator is not used	External input f_{CL}	$f_{CL}/(2\times33)$

Common Output Control Circuit

This circuit controls the relationship between the number of common output and specified duty ratio. Common output mode select instruction specifies the scanning direction of the common output pads.

Table 7

Duty	Status	Common output pads							
		COM [0-15]	**COM [16-23]**	**COM [24-26]**	**COM [27-36]**	**COM [37-39]**	**COM [40-47]**	**COM [48-63]**	**COMS**
1/33	Normal	COM[0-15]	NC					COM[16-31]	COMS
	Reverse	COM[31-16]	NC					COM[15-0]	
1/49	Normal	COM[0-23]		NC			COM[24-47]		COMS
	Reverse	COM[47-24]		NC			COM[23-0]		
1/55	Normal	COM[0-26]			NC	COM[27-53]			COMS
	Reverse	COM[53-27]			NC	COM[26-0]			
1/65	Normal	COM[0-63]							COMS
	Reverse	COM[63-0]							

This is a 197-channel multiplexes that generate voltage levels for driving the liquid crystal. The combination of the display data, the COM scan signal, and the FR signal produces the liquid crystal drive voltage output.
Figure 6 shows example of the SEG and COM output wave form.

Configuration Setting

The NT7502 can be optional into two configuration by DUTY0, DUTY1

DUTY1, DUTY0	Common	Segment	V1	V2	V3	V4
1, 1	65	132	8/9V0, 6/7V0	7/9V0, 5/7V0	2/9V0, 2/7 V0	1/9V0, 1/7V0
1, 0	55	132	7/8V0, 5/6V0	6/8V0, 4/6V0	2/8V0, 2/6 V0	1/8V0, 1/6V0
0, 1	49	132	7/8V0, 5/6V0	6/8V0, 4/6V0	2/8V0, 2/6 V0	1/8V0, 1/6V0
0, 0	33	132	5/6V0, 4/5V0	4/6V0, 3/5V0	2/6 V0, 2/5V0	1/6V0, 1/5V0

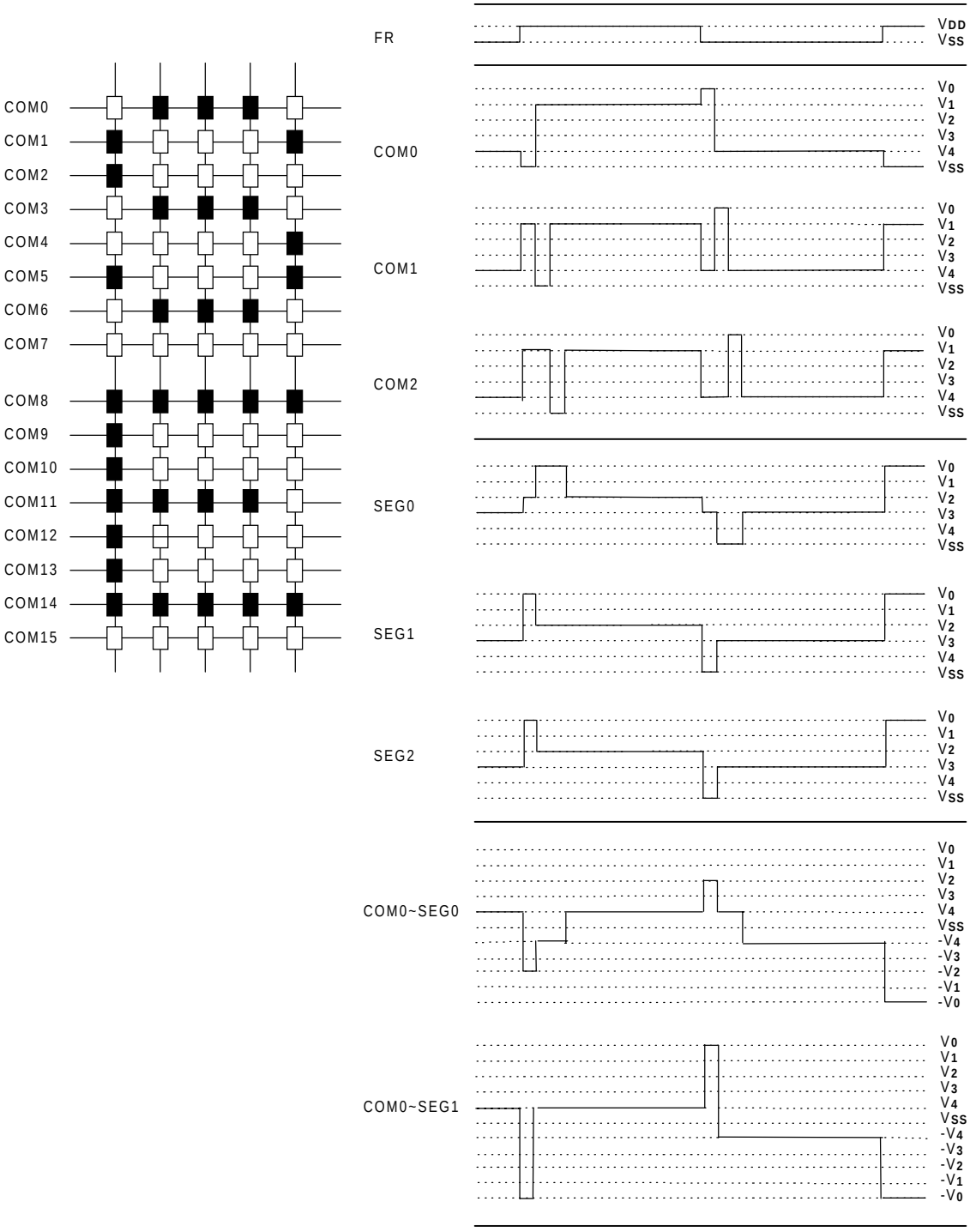

COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10
COM11
COM12
COM13
COM14
COM15
FR
VDD
VSS
COM0
V0
V1
V2
V3
V4
VSS
COM1
V0
V1
V2
V3
V4
VSS
COM2
V0
V1
V2
V3
V4
VSS
SEG0
V0
V1
V2
V3
V4
VSS
SEG1
V0
V1
V2
V3
V4
VSS
SEG2
V0
V1
V2
V3
V4
VSS
COM0~SEG0
V0
V1
V2
V3
V4
VSS
-V4
-V3
-V2
-V1
-V0
COM0~SEG1
V0
V1
V2
V3
V4
VSS
-V4
-V3
-V2
-V1
-V0

Figure 6

The Power Supply Circuit

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the liquid crystal drivers. They comprise Booster circuits, voltage regulator circuits, and voltage follower circuits. They are only enabled in master operation.
The power supply circuits can turn the Booster circuits, the voltage regulator circuits, and the voltage follower circuits ON or OFF independently through the use of the Power Control Set command. Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel. Table 7 shows the Power Control Set Command 3-bit data control function, and Table 8 shows reference combinations.

Table 8 The Control Details of Each Bit of the Power Control Set Command

Item	Status "1"	Status "0"
D2 Booster circuit control bit	ON	OFF
D1 Voltage regulator circuit (V regulator circuit) control bit	ON	OFF
D0 Voltage follower circuit (V/F circuit) control bit	ON	OFF

Table 9

Use Settings	D2	D1	D0	Step-up circuit	Voltage regulator circuit	V/F circuit	External voltage input	Step-up voltage system terminal
1.Only the internal power supply is used	1	1	1	O	O	O	V_{DD2}	Used
2.Only the V regulator circuit and the V/F circuit are used	0	1	1	X	O	O	V_{OUT}, V_{DD2}	Open
3.Only the V/F circuit is used	0	0	1	X	X	O	V_0, V_{DD2}	Open
4.Only the external power supply is used	0	0	0	X	X	X	V_0 to V_4	Open

*The "step-up system terminals" refer CAP1+, CAP1-, CAP2+, CAP2-and CAP3+,
*While other combinations, not shown above, are also possible, these combinations are nor recommended because they have no practical use.

The Step-up Voltage Circuits
Using the step-up voltage circuits equipped within the NT7502 chips it is possible to product 4X，3X，2X Step-up of the V_{DD2}-V_{SS} voltage levels

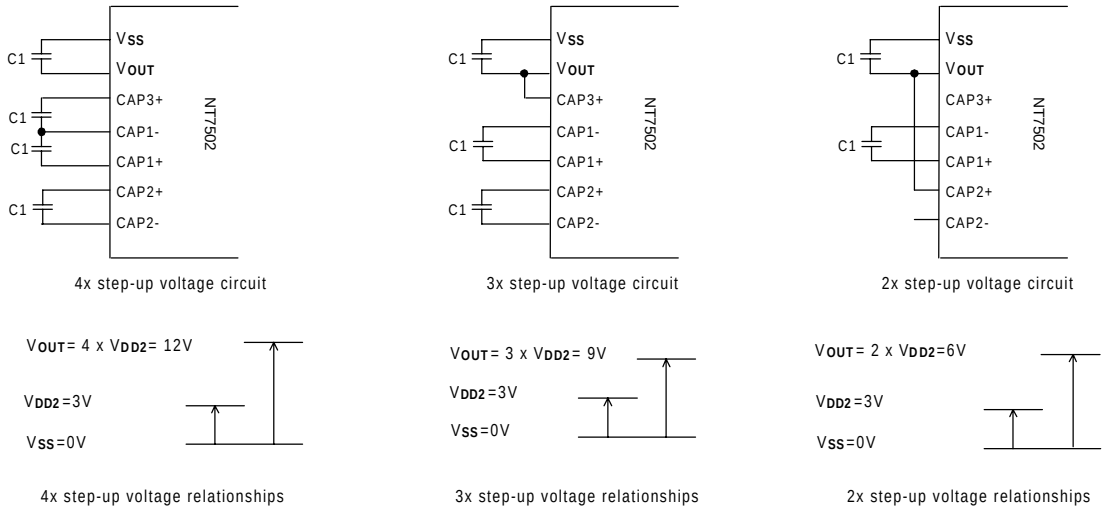


Figure 7

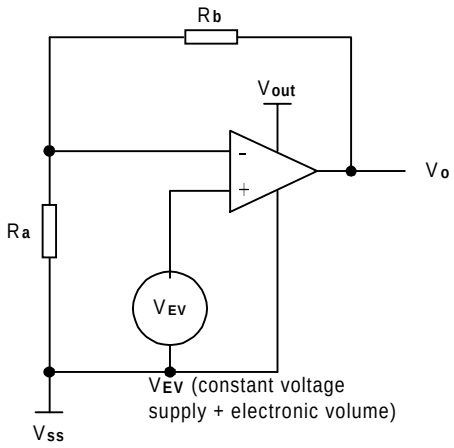
The Voltage regulator circuit

The step-up voltage generated at VOUT outputs the liquid crystal driver voltage V0 through the voltage regulator circuit Because the NT7502 chips have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V0 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components.
Moreover, in the NT7502, three types of thermal gradients have been prepared as VREG options: (1) approximately –0.05%/℃ (2) approximately –0.2%/℃, and (3) external input (supplied to the V_{RS} terminal).

When the V0 Voltage Regulator Internal Resistors Are Used

Through the use of the V0 voltage regulator internal resistors and the electronic volume function the liquid crystal power supply voltage V0 can be controlled by commands alone (without adding any external resistors), making it possible to adjust the liquid crystal display brightness. The V0 voltage can be calculated using equation A-1 over the range where $|V0| < |V_{OUT}|$.

$$V0 = (1+Rb/Ra)*V_{EV} = (1+Rb/Ra)* (1-(63-\alpha)/162)*V_{REG} \quad \text{(Equation A-1)}$$



V_{REG} is the IC internal fixed voltage supply, and its voltage at Ta = 25℃ is as shown in Table 10.

Table 10

Equipment Type	TMPS	VRS	Thermal Gradient	Units	V_{REG}
Internal power Supply	0	1	-0.05	%/℃	2.1
Internal power Supply	1	1	-0.2	%/℃	2.1
External input	*	0	-	-	V_{RS}

α is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume register. Table 10 shows the value for α depending on the electronvolume register settings. Ra/Rb is the V0 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V0 voltage regulator internal resistor ratio set command. The (1+Rb/Ra) retio assumes the values shown in Table11 depending on the 3-bit data settings in the V0 voltage regulator internal resistor ratio register.

Table 11

D5	D4	D3	D2	D1	D0	α	V_0
0	0	0	0	0	0	0	Minimum
0	0	0	0	0	1	1	:
0	0	0	0	1	0	2	:
		:			:	:	:
1	0	0	0	0	0	32 (default)	:
		:			:	:	:
1	1	1	1	1	0	62	:
1	1	1	1	1	1	63	Maximum

V0 voltage regulator internal resistance ratio register value and (1+R_b/R_a) ratio (Reference value)

Table 12

Register			Equipment Type by Thermal Gradient [Units:%/ ℃]		
D2	D1	D0	1. –0.05	2. –0.2	3. V_{REG} External Input
0	0	0	3.0	3.0	1.5
0	0	1	3.5	3.5	2.0
0	1	0	4.0	4.0	2.5
0	1	1	4.5	4.5	3.0
1	0	0	5.0	5.0	3.5
1	0	1	5.5	5.5	4.0
1	1	0	6.0	6.0	4.5
1	1	1	6.4	6.4	5.0

The V0 voltage as a function of the V0 voltage regulator internal resistor ratio register and the electronic volumn register. Setup example: When selecting T_a=25℃ and V0=7V for an NT7502 model on which Temperature gradient=-0.05%/℃ the equation A-1, the following setup is enabled.

Table 13

Contents	Register					
	D5	D4	D3	D2	D1	D0
For V0 voltage regulator	-	-	-	0	1	0
Electronic Volume	1	0	0	1	0	1

- When the V0 voltage regulator internal resistors or the electronic volume function is used, it is necessary to at least set the voltage regulator circuit and the voltage follower circuit to an operating mode using the power control set commands. Moreover, it is necessary to provide a voltage from VOUT when the Booster circuit is OFF.
- The VR terminal is enabled only when the V0 voltage regulator internal resistors are not used (i.e. the IRS terminal="L"). When the V0 voltage regulator internal resistors are used (i.e. when the IRS ternimal ="H"), then the VR terminal is left open.
- Because the input impedance of the VR terminal is high, it is necessary to take into consideration short leads, shield cables,etc. to hadle noise..

The Liquid Crystal Voltage Generator circuit

The V0 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V1, V2, V3, and V4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V1, V2,V3, and V4 to the liquid crystal drive circuit. 1/9 bias or 1/7 bias for NT7502 can be selected.

High Power Mode

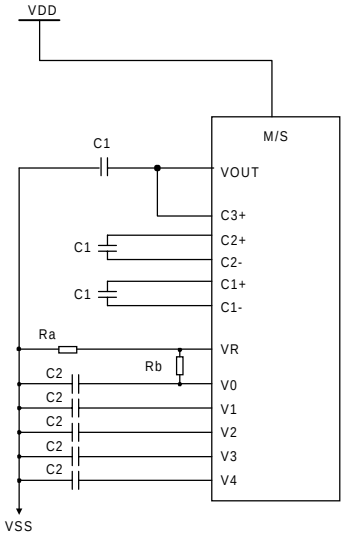
The power supply circuit equipped in the NT7502 chips has very low power consumption (normal mode: $\overline{HPM}$ ="H"). However for LCDs or panels with large loads, this low-power power supply may cause display quality to degrade. When this occurs, setting the $\overline{HPM}$ terminal to "L"(high power mode) can improve the quality of the display. We recommend that the display be checked on actual equipment to determine whether or not to use this mode.

Moreover, if the improvement to the display is inadequate even afterhigh power mode has been set, then it is necessary to adda Command Sequence when Built-in Power Supply is turned OFF

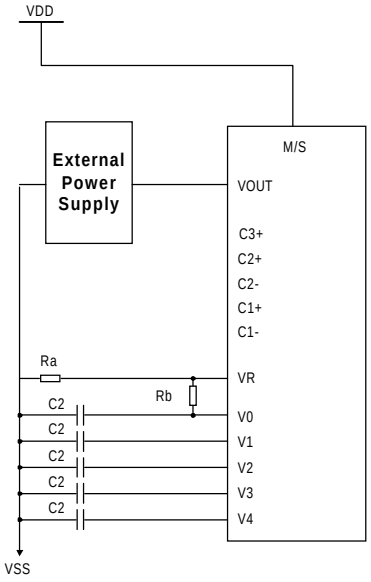
To turn off the built-in power supply, follow the command sequence as shown below to turn it off after making the system into the standby mode.

Reference power supply circuit for driving LCD panel

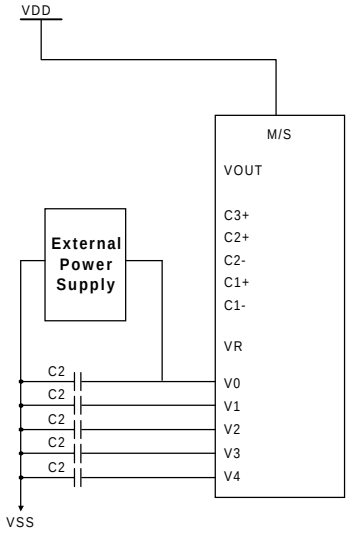
-When using all LCD power circuits
(Voltage converter regulator and follower)
(In case of 3X boosting circuit)



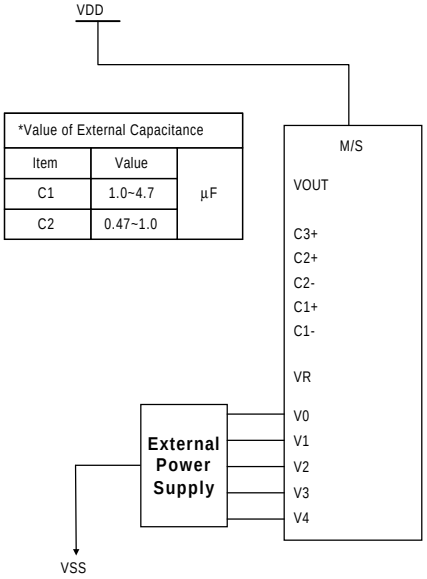
-When not using voltage booster circuits



When only using voltage follower



When not using internal LCD power supply circuits



Reset Circuit

When the $\overline{RES}$ input falls to “L”, these LS1s reenter their default state. The default settings are shown below:

1. Display OFF
2. Normal display
3. ADC select: Normal display (ADC command D0= “L”)
4. Power control register (D2, D1, D0)=(0, 0, 0,)
5. Read modify write OFF
6. Register data clear in serial interface
7. LCD power supply bias ratio 1/9 (1/65 duty), 1/8 (1/55, 1/49 duty) , 1/6 (1/33 duty)
8. Static indicator: OFF
   Static indicator register: (D1, D2)=(0, 0)
9. Display start line register set at first line
10. Column address counter set at address0
11. Page address register set at page 0
12. Common output status normal
13. V0 voltage regulator internal power supply ratio set mode clear:
    V0 voltage regulator internal resistor ratio register: (D2, D1, D0)=(1, 0, 0)
14. Electronic volume register set mode clear
    Electronic volume register: (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0,)
15. Test mode clear
16. All-indicator-lamps-on OFF (All-indicator-lamps ON/OFF command D0=”L”).
17. Output condition of COM, SEG
    COM: V1
    SEG: V2

On the other hand, when the reset command is used only default settings 7 to 15 above are put into effect.

As is described in “11. The MPU interface (Refence Example),” the $\overline{RES}$ terminal is connected to the MPU reset terminal, making the chip reinitialize siumltaneousy with the MPU. At the time of power up, it is necessary to reinitialize using the $\overline{RES}$ ter,oma;. Moreove, when the contro signal from the MPU is in a high impedance state, there may be an overcurrent condition to take measures to prevent the input terminal from entering a high impedance state.

In the NT7502, if the internal liquid crystal power supply circuit is not used, then it is necessary to apply a “L” signal to the $\overline{RES}$ terminal when the external liquid crystal power supply is applied.

Even though the oscillator circuit operates while the $\overline{RES}$ terminal is “L”, the display timing generator circuit is stopped, and the FR, FRS, and $\overline{DOF}$ terminals are fixed to “H” and the CL pin is fixed to “H” only when the intermal oscillator circuit is used. There is no influence on the D0 to D7 terminals.

COMMANDS

The NT7502 uses a combination of A0, $\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only regardless of external clock, its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters a read status when a low pulse is input to the $\overline{RD}$ pad and a write status when a low pulse is input to the $\overline{WR}$ pad. The 6800 series microprocessor interface enters a read status when a high pulse is input to the R/$\overline{W}$ pad and a write status when a low pulse is input to this pad. When a high pulse is input to the E pad, the command is activated. (For timing, see AC Characteristics.). Accordingly, in the command explanation and command table, $\overline{RD}$ (E) becomes 1(high) when the 6800 series microprocessor interface reads status of display data. This is an only different point from the 8080 series microprocessor interface.
Taking the 8080 series, microprocessor interface as an example commands will be explained below.
When the serial interface is selected, input data starting from D7 in sequence.

Command set

1. Display ON/OFF

   Alternatively turns the display on and off.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

   When the display OFF command is executed when in the display all points ON mode, power saver mode is entered. See the section on the power saver for details.

2. Set Display Start Line

   Specifies line address (refer to Figure 4) to determine the initial display line, or COM0. The RAM display data becomes the top line of LCD screen. It is followed by the higher number of lines in ascending order, corresponding to the duty cycle. When this command changes the line address, the smooth scrolling or page change takes place.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

← High-order bit

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
			:			:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

3. Set Page Address

Specifies page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed. Page address 8 is the display RAM area dedicate to the indicator, and only D0 is valid for data change.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Page address
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

4. Set Column Address

Specifies column address of display RAM. Divide the column address into 4 higher bits and 4 lower bits. Set each of them succession. When the microprocessor repeats to access to the display RAM, the column address counter is incremental by during each access until address 132 is accessed. The page address is not changed during this time.

	A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Higher bits	0	1	0	0	0	0	1	A7	A6	A5	A4
Lower bits	0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				:				:
1	0	0	0	0	0	1	1	131

5. Read Status

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Busy: When high, the NT7502 is busy due to internal operation or reset. Any command is rejected until BUSY goes low. The busy check is not required if enough time is provided for each cycle.

ADC: Indicates the relationship between RAM column address and segment drivers. When low, the display is reversed and column address "132-n" corresponds to segment driver n. When high, the display is normal and column address corresponds to segment driver n.

ON/OFF: Indicates whether the display is on or off. When goes low the display turns on. When goes high, the display turns off. This is the opposite of Display ON/OFF command

RESET: Indicates the initialization is in progress by $\overline{RES}$ signal or by reset command. When low, the display is on. When high, the chip is being reset.

6. Write Display Data

Write 8-bit data in display RAM. As the column address is incremental by 1 automatically after each write, the microprocessor can continue to write data of multiple words.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

7. Read Display Data

Reads 8-bit data from display RAM area specified by column address and page address. As the column address is increment by 1 automatically after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

8. ADC Select

Changes the relationship between RAM column address and segment driver. The order of segment driver output pads can be reversed by software. This allows flexible IC layout during LCD module assembly. For details, refer to the column address section of Figure4. When display data is written or read, the column address is incremental by 1 as shown in Figure4.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

When D is low, the right rotation (normal direction).
When D is high, the left rotation (reverse direction).

9. Normal/ Reverse Display

Reverses the Display ON/OFF status without rewriting the contents of the display data RAM.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

When D is low, the RAM data is high, being LCD ON potential (normal display)
When D is high, the RAM data is low, being LCD ON potential (reverse display)

10. Entire Display ON

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.
This command has priority over the Normal/Reverse Display command. When D is low, the normal display status is provided.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D is high, the entire display ON status is provided. If the Entire Display ON command is executed in the display OFF status, the LCD panel enters Power Save mode. Refer to the Power Save section for details.

11. Set LCD Bias

This command selects the voltage bias ratio required for the liquid crystal display.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Duty			
											1/33	1/49	1/55	1/65
0	1	0	1	0	1	0	0	0	1	0	1/6 bias	1/8 bias	1/8 bias	1/9 bias
										1	1/5 bias	1/6 bias	1/6 bias	1/7 bias

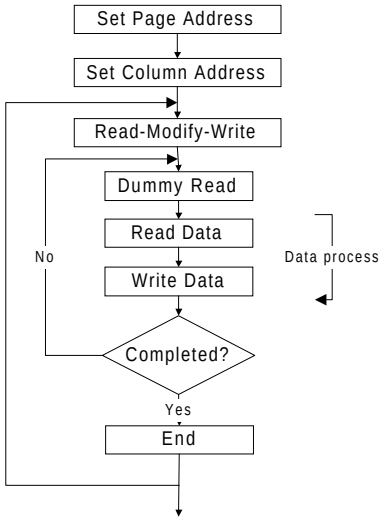
12. Read-Modify-Write

A pair of Read-Modify-Write and End commands must always be used. Once Read-Modify-Write is issued, column address is not incremental by Read Display Data command but incremental by Write Display Data command only. It continues until End command is issued. When the End is issued, column address returns to the address when Read-Modify-Write was issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Note: Any command except Read/Write Display Data and Set Column Address can be issued during Read-Modify-Write mode.

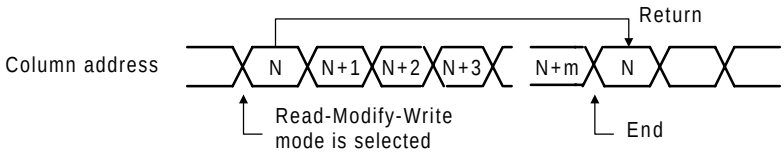
Cursor display sequence



13. End

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write was issued.)

A0	$\overline{E}$ / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0



14. Reset

Resets the Initial Display Line register, Column Address counter, Page Address register, and output status selector circuit to their initial status. The Reset command does not affect on the contents of display RAM. Refer to the Reset circuit section of Function Description.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The Reset command cannot initialize LCD power supply. Only the Reset signal to the $\overline{RES}$ pad can initialize the supplies.

15. Output Status Select Register

Applicable to the NT7502. When D is high or low, the scan direction of the COM output pad is selectable. Refer to Output Status Selector Circuit in Function Description for details.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	D	*	*	*

D : Selects the scan direction of COM output pad
D=0: Normal (COM0 → COM63/53/47/31) D=1: Reverse (COM63/53/47/31 → COM0)
*: Invalid bit

16. Set Power Control

Selects one of eight power circuit functions using 3-bit register. An external power supply and part of on-chip power circuit can be used simultaneously. Refer to Power Supply Circuit section of FUNCTIONAL DESCRIPTION for details.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	A2	A1	A0

When A0 goes low, voltage follower turns off. When A0 goes high, it turns on.
When A1 goes low, voltage regulator turns off. When A1 goes high, it turns on
When A2 goes low, voltage booster turns off. When A2 goes high, it turns on.

17. V0 Voltage Regulator Internal Resistor Ratio Set

This command sets the V0 voltage regulator internal resistor ratio. For details, see the function explanation is “The Power Supply Circuits”.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Rb / Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
									:		:
								1	1	0	
								1	1	1	Large

18. The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal drive voltage V0 through the output from the voltage regulator circuits of the internal liquid crystal power supply.

This command is a two byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

- The Electronic Volume Mode Set

When this command is input, the electronic volume register set command becomes enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

A0	**E** $\overline{RD}$	R / $\overline{W}$ $\overline{WR}$	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	0	0	0	0	0	0	1

- Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal voltage V_o assumes one of the 64 voltage levels.

When this command is input, the electronic volume mode is released after the electronic volume register has been set.

A0	E $\overline{RD}$	R / $\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Rb / Ra Ratio
0	1	0	*	*	0	0	0	0	0	1	Small
0	1	0	*	*	0	0	0	0	1	0	
0	1	0	*	*	0	0	0	0	1	1	
0	1	0	*	*			:				:
0	1	0	*	*	1	1	1	1	1	0	
0	1	0	*	*	1	1	1	1	1	1	Large

When the electronic volume function is not used, set the D5 – D0 to 100000.

19. Static Indicator (Double Byte Command)

This command controls the static drive system indicator display. The static indicator display is controlled by this command only, and is independent of other display control commands.

This is used when one of the static indicator liquid crystal drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal. A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes.

The static indicator ON command is a double byte command paired with the static indicator register set command, and thus one must execute one after the other. (The static indicator OFF command is a single byte command.)

- Static Indicator ON/OFF

When the static indicator ON command is entered, the static indicator register set command is enabled. Once the static indicator ON command has been entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

A0	**E** $\overline{RD}$	R / $\overline{W}$ $\overline{WR}$	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	0	1	0	1	1	0	D

D=0: Static Indicator OFF D=1: Static Indicator ON

■ Static Indicator Register Set

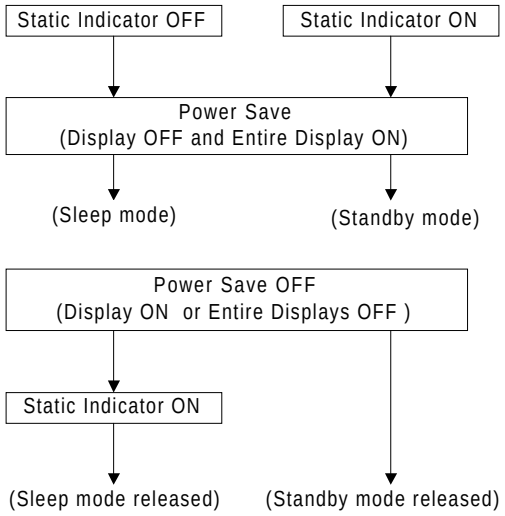
This command sets two bits of data into the static indicator register and is used to set the static indicator into a blinking mode.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Indicator display state
0	1	0	*	*	*	*	*	*	0	0	OFF
									0	1	ON (blinking at approximately 0.5 second intervals
									1	0	ON (blinking at approximately 1 second intervals
									1	1	ON (constantly on)

* Disabled bit

20. Power Save (Compound Command)

When all displays are turned on during display off, the Power Save command is issued to greatly reduce the current consumption.
If the static indicators are off, the Power Save command sleeps the system. If on, this command stands by the system.
Release the Sleep mode using the both Power Save OFF command (Display ON command or Entire Display OFF command) and Set Indicator on command.



Sleep mode

This mode stops every operation of the LCD display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

(1) Stops the oscillator circuit and LCD power supply circuit.
(2) Stops the LCD drive and outputs the Vss level as the segment/common driver output.
(3) Holds the display data and operation mode provided before the start of the sleep mode.
(4) The MPU can access to the built-in display RAM.

Standby mode

Stops the operation of the duty LCD display system and turns on only the static drive system to reduce current consumption to the minimum level required for static drive.

The ON operation of the static drive system indicates that the NT7502 is in the standby mode. The internal status in the standby mode is as follows:

(1) Stop the LCD power supply circuit.
(2) Stop the LCD drive and outputs the Vss level as the segment/common driver output. However, the static drive system operates.
(3) Holds the display data and operation mode provided before the start of the standby mode.
(4) The MPU can access to the built-in display RAM.
When the RESET command is issued in the standby mode, the sleep mode is set.

- When the LCD drive voltage level is given by an external resistive driver, the current of this resistor must be cut so that it may be fixed to floating or Vss level, prior to or concurrently with causing the NT7502 to go to the sleep mode or standby mode.
- When an external power supply is used, likewise, the function of this external power supply must be stopped so that it may be fixed to floating or Vss level, prior to or concurrently with causing the NT7502 to go to the sleep mode or standby mode.

21. NOP

Non-Operation Command

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

22. Test Command

This is the dedicate IC chip test command. It must not be used for normal operation. If the Test command is issued unconsciously, set the $\overline{RES}$ input to low or issue the Reset command to release the test mode.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*

*: Invalid bit

Cautions: The NT7502 holds an operation status specified by each command. However, the internal operation status may be changed by a high level of ambient noise. It must be considered to suppress the noise on the its package and system or to prevent an ambient noise insertion. To prevent a spike noise, a built-in software for periodical status refreshment is recommended to use.
The test command can be inserted in an unexpected place. Therefore it is recommended to enter the test mode reset command F0h during the refresh sequence.

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	D	Turns on LCD panel when goes high, and turns off when goes low
(2) Set Display Start Line	0	1	0	0	1	Display start address						Specifies RAM display line for COM0
(3) Set Page Address	0	1	0	1	0	1	1	Page address				Sets the display RAM page in Page Address register
(4) Set Column Address 4 higher bits	0	1	0	0	0	0	1	Higher column address				Sets 4 higher bits of column address of display RAM in register
(4) Set column Address 4 lower bits	0	1	0	0	0	0	0	Lower column address				Sets 4 lower bits of column address of display RAM in register
(5) Read Status	0	0	1	Status				0	0	0	0	Reads the status information
(6) Write Display Data	1	1	0	Write data								Writes data in display RAM
(7) Read Display Data	1	0	1	Read data								Reads data from display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	D	Sets the display RAM address SEG output correspondence
(9) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	D	Normal indication when low, but full indication when high
(10) Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Selects normal display (0) or Entire Display ON (1)
(11) Set LCD Bias	0	1	0	1	0	1	0	0	0	1	D	Sets LCD drive voltage bias ratio
(12) Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Increments Column Address counter during each write
(13) End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read-Modify-Write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Resets internal functions
(15) Common output mode select	0	1	0	1	1	0	0	D	*	*	*	Selects COM output scan direction. * Invalid data
(16) Set Power Control	0	1	0	0	0	1	0	1	Operation status			Selects the power circuit operation mode
(17) V0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio (Rb / Ra) mode
(18) Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1	Set the V0 output voltage electronic volume register
Electronic Volume Register set	0	1	0	*	*	Electronic control value						
(19) Set static indicator On/Off	0	1	0	1	0	1	0	1	1	0	D	Set static indicator On/Off 0: OFF 1: ON
Set Static indicator register	0	1	0	*	*	*	*	*	*	Mode		Set the flashing mode
(20) Power Save	-	-	-	-	-	-	-	-	-	-	-	Compound command of display OFF and entire display ON
(21) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(22) Test Command	0	1	0	1	1	1	1	*	*	*	*	IC Test command. Do not use!
(23) Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	Command of test mode reset

Note: Do not use any other command, or the system malfunction may result.

Absolute Maximum Rating*

DC Supply Voltage (V_{DD}, V_{DD2}) . . . . . -0.3V to +6.0V

DC Supply Voltage (V_{LCD}, V_0) . . . . -0.3V to +12V

Input Voltage . . . . . -0.3V to V_{DD}+0.3V

Operating Ambient Temperature . . . . . -40°C to +85°C

Storage Temperature . . . . . -55°C to +125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

DC Characteristics (V_{SS}= 0V, V_{DD} = 2.7 - 3.3V T_A = -40 to 85°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{DD}	Operating Voltage	2.4		3.5	V	
V_{DD2}	Operating Voltage	2.4		3.5	V	
V_{OUT}	Booster output voltage	6.0		12.0	V	
V_0	Voltage regulator operation voltage	4.5		11.5	V	
V_{REG1}	Reference voltage	2.04	2.10	2.16	V	T_A=25°C, -0.05%/ °C
V_{REG2}	Reference voltage	2.00	2.10	2.20	V	T_A=25°C, -0.2%/ °C
I_{DD1}	Dynamic current consumption 1	-	21	35	µA	V_{DD} = 3V, V_0 = 11V, build-in power supply off, display on, display data = checker and no access, T_A = 25°C
I_{DD2}	Dynamic current consumption 2	-	96	160	µA	4X boosting, V_{DD}, V_{DD2}=3V, V_0 = 11V, build-in power supply on, display on, display data = checker and no access, T_A = 25°C, temperature gradient is –0.05%/ °C, when V0 voltage internal resistor is used. Normal mode
I_{DD3}	Dynamic current consumption 3	-	153	255	µA	4X boosting, V_{DD}, V_{DD2}=3V, V_0 = 11V, build-in power supply on, display on, display data = checker and no access, T_A = 25°C, temperature gradient is –0.05%/ °C, when V0 voltage internal resistor is used. High power mode
I_{SP}	Sleep mode current consumption		0.01	5	µA	During sleep, T_A = 25°C
I_{SB}	Standby mode current consumption		4	8	µA	During standby, T_A = 25°C
V_{IHC}	High-level input voltage	0.8× V_{DD}		V_{DD}	V	A0, D0 - D7, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CLS, CL, FR, M/S, C86, P/S, $\overline{DOF}$, $\overline{RES}$, TMPS, VRS, IRS, and $\overline{HPM}$
V_{ILC}	Low-level input voltage	V_{SS}		0.2× V_{DD}	V	
V_{OHC}	High-level output voltage	0.8× V_{DD}		V_{DD}	V	I_{OH}=-0.5mA (D0 – D7, FR, FRS, $\overline{DOF}$, and CL)
V_{OLC}	Low -level output voltage	V_{SS}		0.2× V_{DD}		I_{OL}=0.5mA (D0 – D7, FR, FRS, $\overline{DOF}$, and CL)
I_{LI}	Input leakage current	-1.0		1.0	µA	V_{IN}=V_{DD} or V_{SS} (A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CLS, M/S, C86, P/S, IRS, TMPS, VRS and $\overline{RES}$)
I_{HZ}	HZ leakage current	-3.0		3.0	µA	When the D0 - D7, FR, CL, and $\overline{DOF}$ are in high impedance

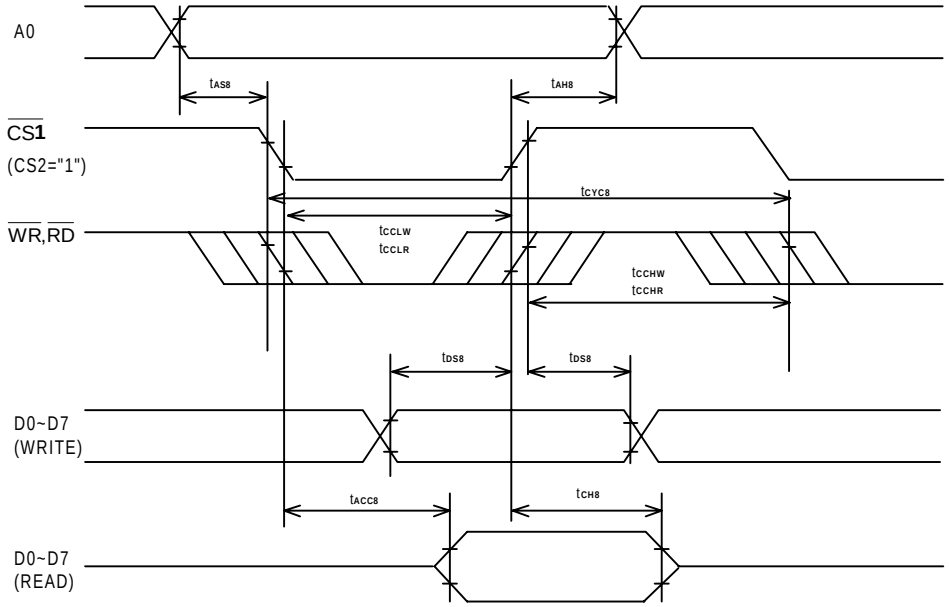
DC Characteristics (Continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
R_{ON1}	LCD driver ON resistance		2.0	3.5	kΩ	V_0= 11.0V	T_A=25°C, These are the resistance values for when a 0.1V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V1, V2, V3, V4).
R_{ON2}	LCD driver ON resistance		3.2	5.4	kΩ	V_0= 8.0V	
C_{IN}	Input pad capacity		5.0	8.0	pF	T_A=25°C, f=1MHz	
f_{OSC}	Oscillation frequency	27	33	39	kHZ	T_A=25°C	

Notes: 1. Voltages $V_0 \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_{SS}$ must always be satisfied.

AC Characteristics

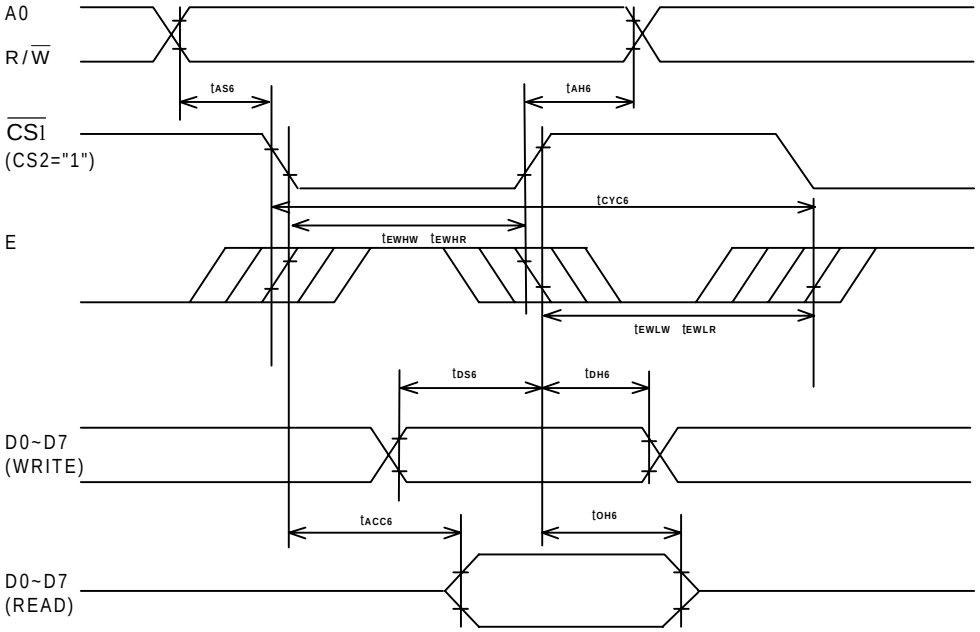
(1) System buses Read/Write characteristics 1 (For the 8080 Series MPU)



(V_{DD}=2.7 – 3.3V, T_A = -40 - 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{AH8}	Address hold time	0			ns	
T_{AS8}	Address setup time	0			ns	
T_{CYC8}	System cycle time	300			ns	
T_{CCLW}	Control L pulse width (WR)	60			ns	
T_{CCLR}	Control L pulse width (RD)	120			ns	
T_{CCHW}	Control H pulse width (WR)	60			ns	
T_{CCHR}	Control H pulse width (RD)	60			ns	
T_{DS8}	Data setup time	40			ns	
7T_{DH8}	Data hold time	15			ns	
T_{ACC8}	$\overline{RD}$ access time			140	ns	C_L=100pF
T_{CH8}	Output disable time	10		100	ns	C_L=100pF

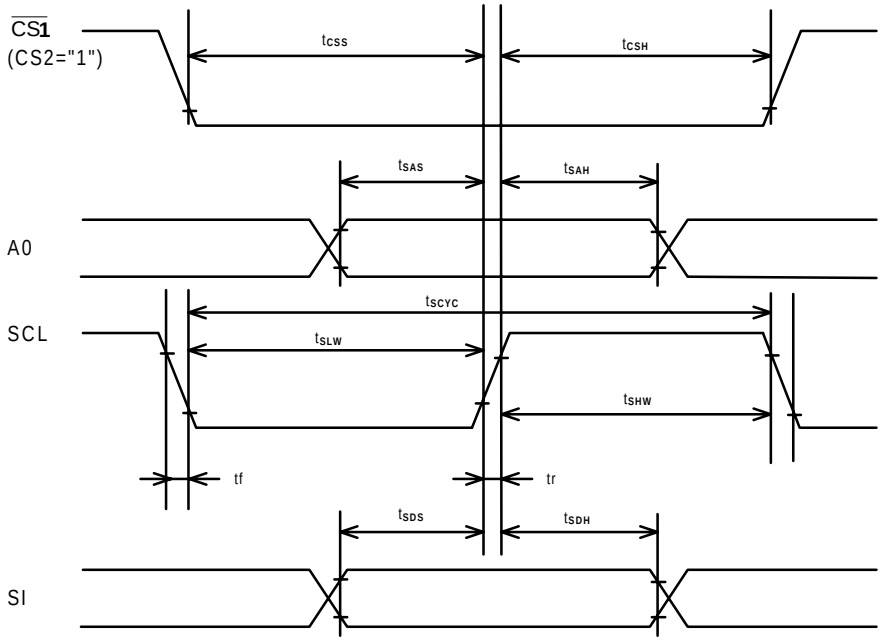
(2) System buses Read/Write Characteristics 2 (6800 Series MPU)



(V_{DD}=2.7 – 3.3V, T_A = -40 - 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{CYC6}	System cycle time	300			nS	
T_{AS6}	Address setup time	0			nS	
T_{AH6}	Address hold time	0			nS	
T_{DS6}	Data setup time	40			nS	
T_{DH6}	Data hold time	15			nS	
T_{OH6}	Output disable time	10		100	nS	C_L=100pF
T_{ACC6}	Access time			140	nS	C_L=100pF
T_{EWHR}	Enable H pulse width (Read)	120			nS	
T_{EWHW}	Enable H pulse width (Write)	60			nS	
T_{EWLR}	Enable L pulse width (Read)	60			nS	
T_{EWLW}	Enable L pulse width (Write)	60			nS	

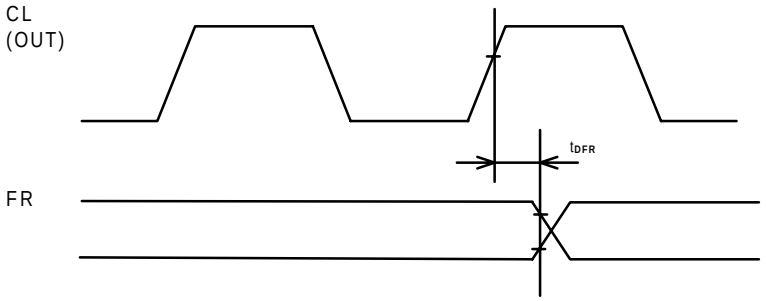
(3) Serial interface



(VDD=2.7 – 3.3V, TA = -40 - 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
TSCYC	Serial clock cycle	250			nS	
TSHW	Serial clock H pulse width	100			nS	
TSLW	Serial clock L pulse width	100			nS	
TSAS	Address setup time	150			nS	
TSAH	Address hold time	150			nS	
TSDS	Data setup time	100			nS	
TSDH	Data hole time	100			nS	
TCSS	$\overline{cs}$ serial clock time	150			nS	
TCSH	$\overline{cs}$ serial clock time	150			nS	

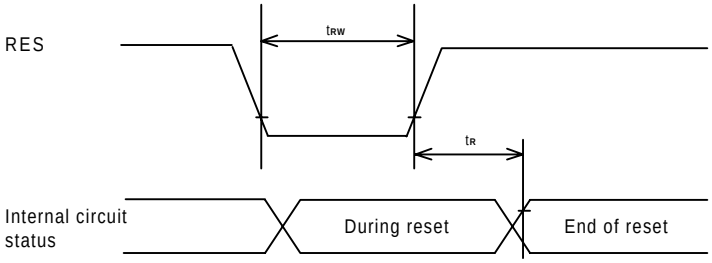
(4) Display control timing



(V_{DD}=2.7 – 3.3V, T_A = -40 - 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{DFR}	FR delay time		20	80	nS	C_L=50pF

(5) Reset timing



(V_{DD}=2.7 – 3.3V, T_A = -40 - 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_R	Reset time			1.0	µS	
T_W	Reset low pulse width	1.0			µS	

MICROPROCESSOR INTERFACE (for reference only)

8080-series microprocessors

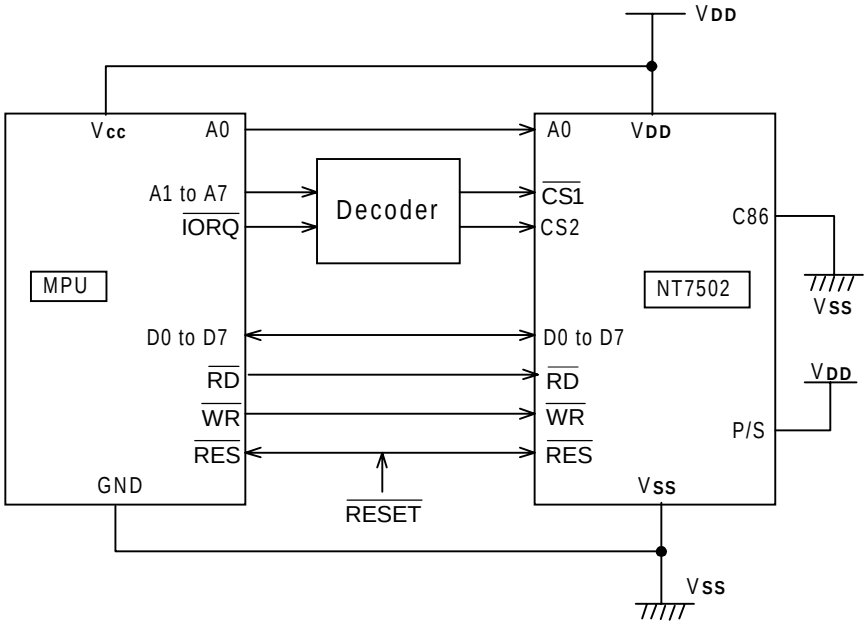


Figure 8

6800-series microprocessors

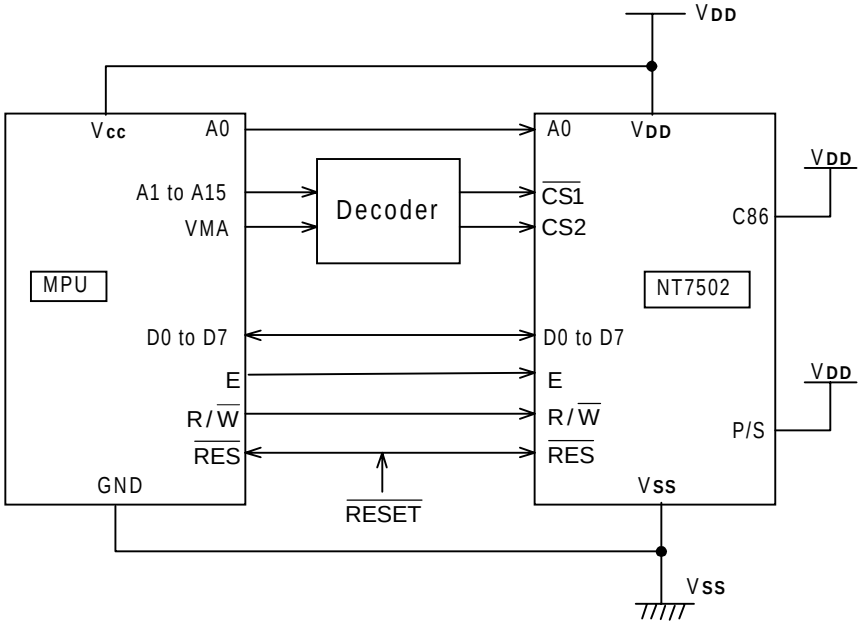
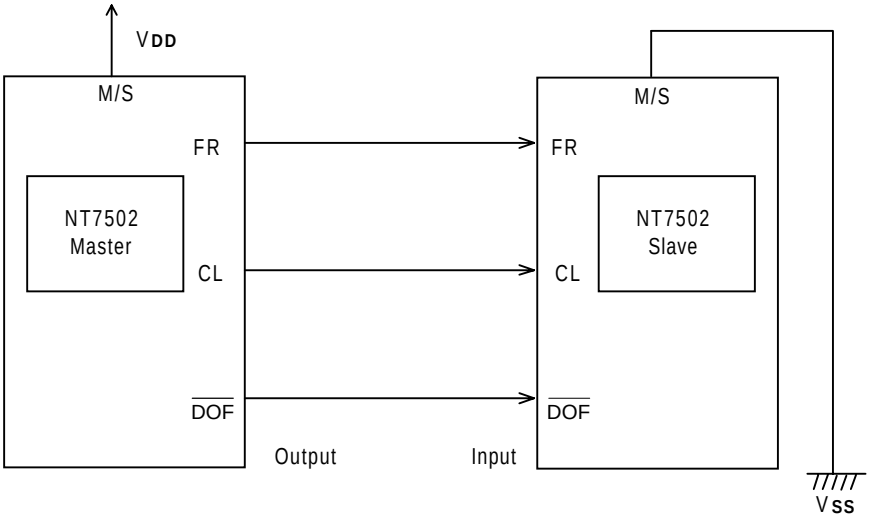


Figure 9

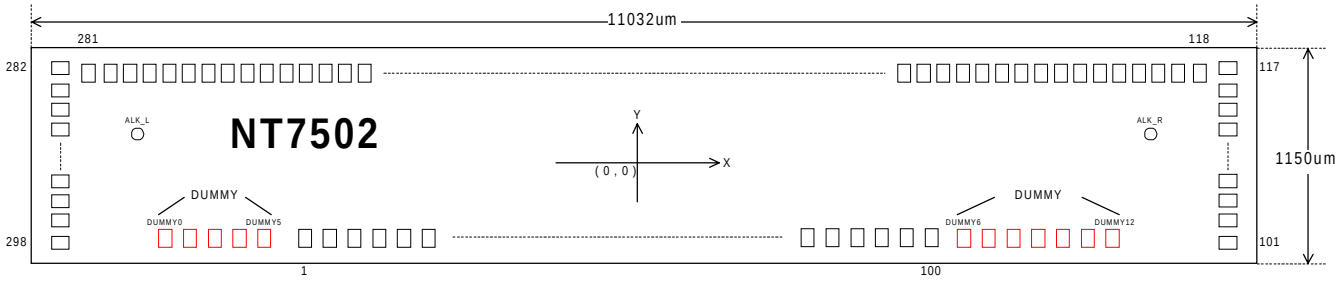
Connections between LCD Drivers (for reference only)

The liquid crystal display area can be enlarged with ease through the use of multiple NT7502 chips. Use a same equipment type.

NT7502 (master) ↔ NT7502 (slave)



Bonding Diagram



Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	NC	-4548.65	-497.5	31	VDD	-1848.65	-497.5
2	FRS	-4458.65	-497.5	32	VDD	-1758.65	-497.5
3	FR	-4368.65	-497.5	33	VDD	-1668.65	-497.5
4	CL	-4278.65	-497.5	34	VDD2	-1578.65	-497.5
5	$\overline{DOF}$	-4188.65	-497.5	35	VDD2	-1488.65	-497.5
6	NC	-4098.65	-497.5	36	VDD2	-1398.65	-497.5
7	VSS	-4008.65	-497.5	37	VSS	-1308.65	-497.5
8	$\overline{CS1}$	-3918.65	-497.5	38	VSS	-1218.65	-497.5
9	CS2	-3828.65	-497.5	39	VSS	-1128.65	-497.5
10	VDD	-3738.65	-497.5	40	VSS	-1038.65	-497.5
11	$\overline{RES}$	-3648.65	-497.5	41	VOUT	-948.65	-497.5
12	A0	-3558.65	-497.5	42	VOUT	-858.65	-497.5
13	VSS	-3468.65	-497.5	43	CAP3+	-768.65	-497.5
14	$\overline{WR}$	-3378.65	-497.5	44	CAP3+	-678.65	-497.5
15	$\overline{RD}$	-3288.65	-497.5	45	CAP1-	-588.65	-497.5
16	VDD	-3198.65	-497.5	46	CAP1-	-498.65	-497.5
17	D0	-3108.65	-497.5	47	CAP1+	-408.65	-497.5
18	D1	-3018.65	-497.5	48	CAP1+	-318.65	-497.5
19	D2	-2928.65	-497.5	49	CAP2+	-228.65	-497.5
20	D3	-2838.65	-497.5	50	CAP2+	-138.65	-497.5
21	D4	-2748.65	-497.5	51	CAP2-	-48.65	-497.5
22	D5	-2658.65	-497.5	52	CAP2-	41.35	-497.5
23	D6	-2568.65	-497.5	53	VDD	131.35	-497.5
24	D7	-2478.65	-497.5	54	VEXT	221.35	-497.5
25	VSS	-2388.65	-497.5	55	VRS	311.35	-497.5
26	VDD	-2298.65	-497.5	56	VSS	401.35	-497.5
27	DUTY0	-2208.65	-497.5	57	V1	491.35	-497.5
28	DUTY1	-2118.65	-497.5	58	V1	581.35	-497.5
29	VSS	-2028.65	-497.5	59	V2	671.35	-497.5
30	VDD	-1938.65	-497.5	60	V2	761.35	-497.5

Bonding Diagram (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
61	V3	851.35	-497.5	101	COM31	5453	-525.6
62	V3	941.35	-497.5	102	COM30	5453	-454.6
63	V4	1031.35	-497.5	103	COM29	5453	-389.6
64	V4	1121.35	-497.5	104	COM28	5453	-324.6
65	V0	1211.35	-497.5	105	COM27	5453	-259.6
66	V0	1301.35	-497.5	106	COM26	5453	-194.6
67	VR	1391.35	-497.5	107	COM25	5453	-129.6
68	VR	1481.35	-497.5	108	COM24	5453	-64.6
69	VSS	1571.35	-497.5	109	COM23	5453	0.4
70	VSS	1661.35	-497.5	110	COM22	5453	65.4
71	VDD	1751.35	-497.5	111	COM21	5453	130.4
72	M/S	1841.35	-497.5	116	COM20	5453	195.4
73	CLS	1931.35	-497.5	113	COM19	5453	260.4
74	VSS	2021.35	-497.5	114	COM18	5453	325.4
75	C86	2111.35	-497.5	115	COM17	5453	390.4
76	P/S	2201.35	-497.5	116	COM16	5453	455.4
77	VDD	2291.35	-497.5	117	COM15	5453	526.4
78	$\overline{\text{HPM}}$	2381.35	-497.5	118	COM14	5303.5	504.45
79	VSS	2471.35	-497.5	119	COM13	5232.5	504.45
80	IRS	2561.35	-497.5	120	COM12	5167.5	504.45
81	VDD	2651.35	-497.5	121	COM11	5102.5	504.45
82	TMPS	2741.35	-497.5	122	COM10	5037.5	504.45
83	VSS	2831.35	-497.5	123	COM9	4972.5	504.45
84	TEST0	2921.35	-497.5	124	COM8	4907.5	504.45
85	NC	3011.35	-497.5	125	COM7	4842.5	504.45
86	TEST1	3101.35	-497.5	126	COM6	4777.5	504.45
87	NC	3191.35	-497.5	127	COM5	4712.5	504.45
88	TEST2	3281.35	-497.5	128	COM4	4647.5	504.45
89	VSS	3371.35	-497.5	129	COM3	4582.5	504.45
90	TEST3	3461.35	-497.5	130	COM2	4517.5	504.45
91	VDD	3551.35	-497.5	131	COM1	4452.5	504.45
92	NC	3641.35	-497.5	132	COM0	4387.5	504.45
93	NC	3731.35	-497.5	133	COMS	4322.5	504.45
94	NC	3821.35	-497.5	134	SEG0	4257.5	504.45
95	NC	3911.35	-497.5	135	SEG1	4192.5	504.45
96	NC	4001.35	-497.5	136	SEG2	4127.5	504.45
97	NC	4091.35	-497.5	137	SEG3	4062.5	504.45
98	NC	4181.35	-497.5	139	SEG4	3997.5	504.45
99	NC	4271.35	-497.5	139	SEG5	3932.5	504.45
100	NC	4361.35	-497.5	140	SEG6	3867.5	504.45

Bonding Diagram (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
141	SEG7	3802.5	504.45	181	SEG47	1202.5	504.45
142	SEG8	3737.5	504.45	182	SEG48	1137.5	504.45
143	SEG9	3672.5	504.45	183	SEG49	1072.5	504.45
144	SEG10	3607.5	504.45	184	SEG50	1007.5	504.45
145	SEG11	3542.5	504.45	185	SEG51	942.5	504.45
146	SEG12	3477.5	504.45	186	SEG52	877.5	504.45
147	SEG13	3412.5	504.45	187	SEG53	812.5	504.45
148	SEG14	3347.5	504.45	188	SEG54	747.5	504.45
149	SEG15	3282.5	504.45	189	SEG55	682.5	504.45
150	SEG16	3217.5	504.45	190	SEG56	617.5	504.45
151	SEG17	3152.5	504.45	191	SEG57	552.5	504.45
152	SEG18	3087.5	504.45	192	SEG58	487.5	504.45
153	SEG19	3022.5	504.45	193	SEG59	422.5	504.45
154	SEG20	2957.5	504.45	194	SEG60	357.5	504.45
155	SEG21	2892.5	504.45	195	SEG61	292.5	504.45
156	SEG22	2827.5	504.45	196	SEG62	227.5	504.45
157	SEG23	2762.5	504.45	197	SEG63	162.5	504.45
158	SEG24	2697.5	504.45	198	SEG64	97.5	504.45
159	SEG25	2632.5	504.45	199	SEG65	32.5	504.45
160	SEG26	2567.5	504.45	200	SEG66	-32.5	504.45
161	SEG27	2502.5	504.45	201	SEG67	-97.5	504.45
162	SEG28	2437.5	504.45	202	SEG68	-162.5	504.45
163	SEG29	2372.5	504.45	203	SEG69	-227.5	504.45
164	SEG30	2307.5	504.45	204	SEG70	-292.5	504.45
165	SEG31	2242.5	504.45	205	SEG71	-357.5	504.45
166	SEG32	2177.5	504.45	206	SEG72	-422.5	504.45
167	SEG33	2112.5	504.45	207	SEG73	-487.5	504.45
168	SEG34	2047.5	504.45	208	SEG74	-552.5	504.45
169	SEG35	1982.5	504.45	209	SEG75	-617.5	504.45
170	SEG36	1917.5	504.45	210	SEG76	-682.5	504.45
171	SEG37	1852.5	504.45	211	SEG77	-747.5	504.45
172	SEG38	1787.5	504.45	212	SEG78	-812.5	504.45
173	SEG39	1722.5	504.45	213	SEG79	-877.5	504.45
174	SEG40	1657.5	504.45	214	SEG80	-942.5	504.45
175	SEG41	1592.5	504.45	215	SEG81	-1007.5	504.45
176	SEG42	1527.5	504.45	216	SEG82	-1072.5	504.45
177	SEG43	1462.5	504.45	217	SEG83	-1137.5	504.45
178	SEG44	1397.5	504.45	218	SEG84	-1202.5	504.45
179	SEG45	1332.5	504.45	219	SEG85	-1267.5	504.45
180	SEG46	1267.5	504.45	220	SEG86	-1332.5	504.45

Bonding Diagram (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
221	SEG87	-1397.5	504.45	261	SEG127	-3997.5	504.45
222	SEG88	-1462.5	504.45	262	SEG128	-4062.5	504.45
223	SEG89	-1527.5	504.45	263	SEG129	-4127.5	504.45
224	SEG90	-1592.5	504.45	264	SEG130	-4192.5	504.45
225	SEG91	-1657.5	504.45	265	SEG131	-4257.5	504.45
226	SEG92	-1722.5	504.45	266	COM32	-4322.5	504.45
227	SEG93	-1787.5	504.45	267	COM33	-4387.5	504.45
228	SEG94	-1852.5	504.45	268	COM34	-4452.5	504.45
229	SEG95	-1917.5	504.45	269	COM35	-4517.5	504.45
230	SEG96	-1982.5	504.45	270	COM36	-4582.5	504.45
231	SEG97	-2047.5	504.45	271	COM37	-4647.5	504.45
232	SEG98	-2112.5	504.45	272	COM38	-4712.5	504.45
233	SEG99	-2177.5	504.45	273	COM39	-4777.5	504.45
234	SEG100	-2242.5	504.45	274	COM40	-4842.5	504.45
235	SEG101	-2307.5	504.45	275	COM41	-4907.5	504.45
236	SEG102	-2372.5	504.45	276	COM42	-4972.5	504.45
237	SEG103	-2437.5	504.45	277	COM43	-5037.5	504.45
238	SEG104	-2502.5	504.45	278	COM44	-5102.5	504.45
239	SEG105	-2567.5	504.45	279	COM45	-5167.5	504.45
240	SEG106	-2632.5	504.45	280	COM46	-5232.5	504.45
241	SEG107	-2697.5	504.45	281	COM47	-5303.5	504.45
242	SEG108	-2762.5	504.45	282	COM48	-5453	526.4
243	SEG109	-2827.5	504.45	283	COM49	-5453	455.4
244	SEG110	-2892.5	504.45	284	COM50	-5453	390.4
245	SEG111	-2957.5	504.45	285	COM51	-5453	325.4
246	SEG112	-3022.5	504.45	286	COM52	-5453	260.4
247	SEG113	-3087.5	504.45	287	COM53	-5453	195.4
248	SEG114	-3152.5	504.45	288	COM54	-5453	130.4
249	SEG115	-3217.5	504.45	289	COM55	-5453	65.4
250	SEG116	-3282.5	504.45	290	COM56	-5453	0.4
251	SEG117	-3347.5	504.45	291	COM57	-5453	-64.6
252	SEG118	-3412.5	504.45	292	COM58	-5453	-129.6
253	SEG119	-3477.5	504.45	293	COM59	-5453	-194.6
254	SEG120	-3542.5	504.45	294	COM60	-5453	-259.6
255	SEG121	-3607.5	504.45	295	COM61	-5453	-324.6
256	SEG122	-3672.5	504.45	296	COM62	-5453	-389.6
257	SEG123	-3737.5	504.45	297	COM63	-5453	-454.6
258	SEG124	-3802.5	504.45	298	COMS	-5453	-525.6
259	SEG125	-3867.5	504.45		ALK_L	5140	200
260	SEG126	-3932.5	504.45		ALK_R	-5140	200

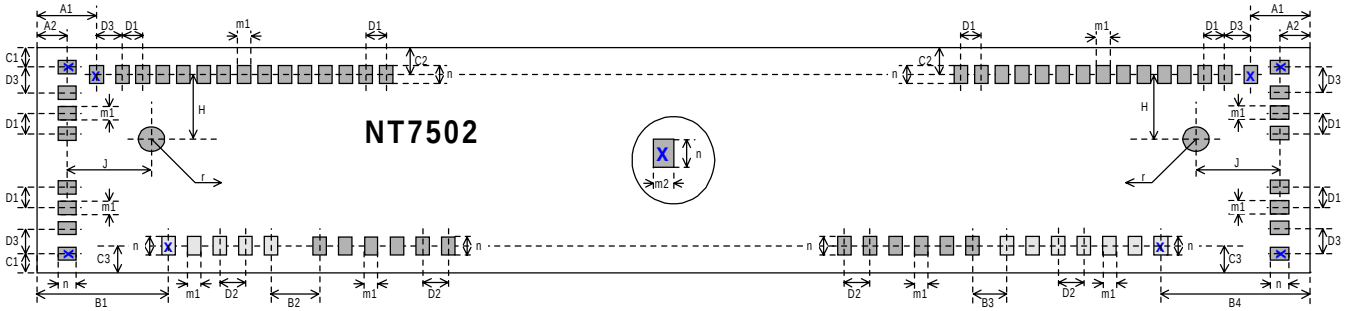
Dummy Pad Location (Total: 12 pads)

NO	X	Y	NO	X	Y	NO	X	Y	NO	X	Y
0	-5060	-497.50	3	-4790	-497.50	6	4550	-497.50	9	4820	-497.50
1	-4970	-497.50	4	-4700	-497.50	7	4640	-497.50	10	4910	-497.50
2	-4880	-497.50	5	4460	-497.50	8	4730	-497.50	11	5000	-497.50

Package Information

Chip Outline Dimensions

unit: inches/um



Symbol	Dimensions in um	Symbol	Dimensions in um
A1	212.5	D1	65
A2	63	D2	90
B1	456	D3	71
B2	151.35	r	35
B3	98.65	H	304.45
B4	516	J	313
C1	48.6	m1	46
C2	70.55	m2	58
C3	77.5	n	90