

433/868/915MHz RF Transceiver with Embedded 8051 Compatible Microcontroller and 4 Input, 10 Bit ADC

nRF9E5

FEATURES

- nRF905 433/868/915 MHz transceiver
- 8051 compatible microcontroller
- 4 input, 10bit 80ksps ADC
- Single 1.9V to 3.6V supply
- Small 32 pin QFN (5x5 mm) package
- Extremely low cost Bill of Material (BOM)
- Internal VDD monitoring
- 2.5µA standby with wakeup on timer or external pin
- Adjustable output power up to 10dBm
- Channel switching time less than 650µs
- Low TX supply current, typical 11mA @-10dBm
- Low RX supply current typical 12.5mA peak
- Low MCU supply current, typ. 1mA at 4MHz @3volt
- Suitable for frequency hopping
- Carrier Detect for "listen before transmit protocol"

APPLICATIONS

- Sports and leisure equipment
- Alarm and security system
- Industrial sensors
- Remote control
- Surveillance
- Automotive
- Telemetry
- Keyless entry
- Toys

GENERAL DESCRIPTION

nRF9E5 is a true single chip system with fully integrated RF transceiver, 8051 compatible microcontroller and a 4 input 10bit 80ksps AD converter. The transceiver of the system supports all the features available in the nRF905 chip including ShockburstTM, which automatically handles preamble, address and CRC. The circuit has embedded voltage regulators, which provides maximum noise immunity and allows operation on a single 1.9V to 3.6V supply. nRF9E5 is compatible with FCC standard CFR47 part 15 and ETSI EN 300 220-1.

QUICK REFERENCE DATA

Parameter	Value	Unit
Minimum supply voltage	1.9	V
Temperature range	-40 to +85	°C
Supply current in transmit @ -10dBm output power	11	mA
Supply current in receive mode	12.5	mA
Supply current for µ-controller 4MHz @ 3volt	1	mA
Supply current for ADC	0.9	mA
Maximum transmit output power	10	dBm
Transmitted data rate (Manchester-encoder embedded)	100	kbps
Sensitivity	-100	dBm
Supply current in power down mode	2.5	µA

Table 1 nRF9E5 quick reference data.



ORDERING INFORMATION

Type number	Description	Version
nRF9E5 IC	32L QFN 5x5 mm	-
nRF9E5-EVKIT 433	Evaluation kit 433MHz	1.0
nRF9E5-EVKIT 868/915	Evaluation kit 868/915MHz	1.0

Table 2 nRF9E5 ordering information.

BLOCK DIAGRAM

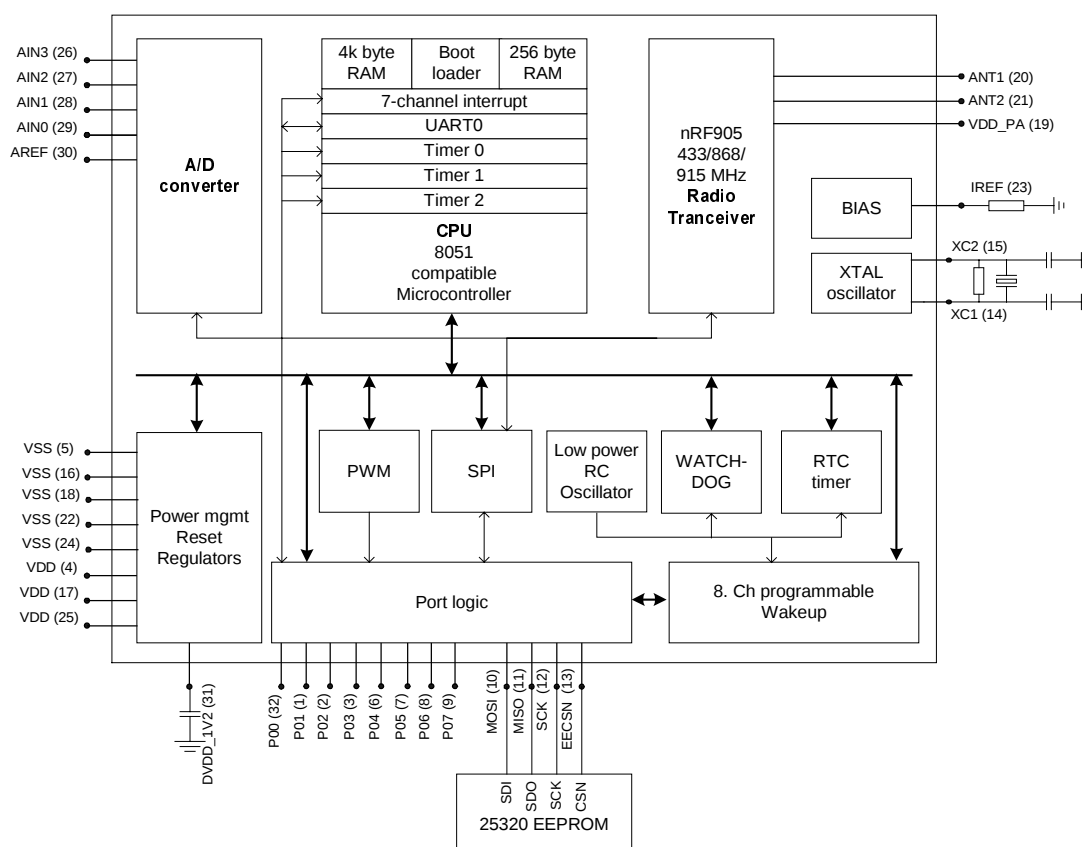


Figure 1 nRF9E5 block diagram.



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1 ARCHITECTURAL OVERVIEW

This section will give a brief overview of each of the blocks in the block diagram in Figure 1.

1.1 Microcontroller

The nRF9E5 microcontroller is instruction set compatible with the industry standard 8051. Instruction timing is slightly different from the industry standard, typically each instruction will use from 4 to 20 clock cycles, compared with 12 to 48 for the “standard”. The interrupt controller is extended to support 5 additional interrupt sources; ADC, SPI, 2 for the radio and a wakeup function. There are also 3 timers that are 8052 compatible, plus some extensions, in the microcontroller core. An 8051 compatible UART that can use timer1 or timer2 for baud rate generation in the traditional asynchronous modes is included. The CPU is equipped with 2 data pointers to facilitate easier moving of data in the XRAM area, which is a common 8051 extension. The microcontroller clock is derived from the crystal oscillator.

1.1.1 Memory Configuration

The microcontroller has a 256-byte data ram (8052 compatible, with the upper half only addressable by register indirect addressing). A small ROM of 512 bytes contains a bootstrap loader that is executed automatically after power on reset or if initiated by software later. The user program is normally loaded into a 4k byte RAM¹ from an external serial EEPROM by the bootstrap loader. The 4k byte RAM may also (partially) be used for data storage in some applications.

1.1.2 Boot EEPROM/FLASH

The program code for the device must be loaded from an external non-volatile memory. The default boot loader expects this to be a “generic 25320” EEPROM with SPI interface. These memories are available from several vendors with supply ranges down to 1.8V. The SPI interface uses the pins MISO (from EEPROM SDO), SCK (to EEPROM SCK), MOSI (to EEPROM SDI) and EECSN (to EEPROM CSN). When the boot is completed, the MISO (P1.2), MOSI (P1.0) and SCK (P1.1) pins may be used for other purposes such as other SPI devices or GPIO (General Purpose Input Output).

1.1.3 Register Map

The SFR (Special Function Registers) control several of the features of the nRF9E5. Most of the nRF9E5 SFRs are identical to the standard 8051 SFRs. However, there are additional SFRs that control features that are not available in the standard 8051.

The SFR map is shown in Table 3. The registers with grey background are registers with industry standard 8051 behavior. Note that the function of P0, P1 and P2 are somewhat different from the “standard” even if the conventional addresses (0x80, 0x90 and 0xA0) are used.

¹ Optionally this 4k block of memory can be configured as 2k mask ROM and 2k RAM or 4 k mask ROM



	X000	X001	X010	X011	X100	X101	X110	X111
F8	EIP						HWREV	
F0	B							
E8	EIE							
E0	ACC							
D8	EICON							
D0	PSW							
C8	T2CON		RCAP2L	RCAP2H	TL2	TH2		
C0								
B8	IP							CKLF CON
B0		RSTREA S	SPI _DATA	SPI _CTRL	SPI CLK	TICK_ DV	CK_ CTRL	TEST_ MODE
A8	IE	PWM CON	PWM DUTY	REGX _MSB	REGX _LSB	REGX _CTRL		
A0	P2							
98	SCON	SBUF						
90	P1	EXIF	MPAGE	P0_DRV	P0_DIR	P0_ALT	P1_DIR	P1_ALT
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	SPC_FNC
80	P0	SP	DPL0	DPH0	DPL1	DPH1	DPS	PCON

Table 3 SFR Register map.

1.2 PWM

The nRF9E5 has one programmable PWM (Pulse-Width Modulation) output, which is the alternate function of P0.7. The resolution of the PWM is software programmable to 6, 7 or 8 bits. The frequency of the PWM signal is programmable via a 6 bit prescaler from the XTAL oscillator. The duty cycle is programmable between 0% and 100% via one 8-bit register.

1.3 SPI

nRF9E5 features a simple single buffered SPI (Serial Programmable Interface) master. The 3 data lines of the SPI bus (MISO, SCK and MOSI) are multiplexed (by writing to register SPI_CTRL) between the GPIO pins (lower 3 bits of P1) and the RF transceiver and AD subsystems. The SPI hardware does not generate any chip select signal. The programmer will typically use GPIO bits (from port P0) to act as chip selects for one or more external SPI devices. The EEC SN pin is a general purpose IO dedicated as chip select for the boot EEPROM. When the SPI interfaces the RF transceiver, the chip selects are available in an internal GPIO port, P2.

1.4 Port Logic

The device has 8 general-purpose bi-directional pins (the P0 port). Additionally the 4 SPI data pins may be used as general purpose IO (the P1). Most of the GPIO pins can be used for multiple purposes under program control. The alternate functions include two external interrupts, UART RXD and TXD, a SPI master port, three enable/count signals for the timers and the PWM output and a slow programmable timer. Each pin in the P0 port can be programmed for high sink or source current.



1.5 Power Management

The nRF9E5 can be placed into several low power modes under program control, and also the ADC and RF subsystems can be turned on or off under program control. The CPU will stop, but all RAM's and registers maintain their values. The watchdog, RTC (Real Time Clock) wakeup timer and the GPIO wakeup function are always active during power down. The current consumption is typically 2.5 μ A when running with the crystal oscillator off.

The device can exit the power down modes by an external pin, an event on any of the P0 GPIO pins, by the wakeup timer if enabled or by a watchdog reset.

1.6 LF Clock, RTC Wakeup Timer, GPIO Wakeup and Watchdog

The nRF9E5 contains an internal low frequency clock CKLF that is always on. When the crystal oscillator clocks the circuit, the CKLF is a 4kHz clock derived from the crystal oscillator. When no crystal oscillator clock is available, the CKLF is a low power RC oscillator that cannot be disabled, so it will run continuously as long as $VDD \geq 1.8V$. The RTC Wakeup timer, the GPIO wakeup and watchdog all run on the CKLF to ensure these vital functions will work during all power down modes.

RTC Wakeup timer is a 24 bit programmable down counter and the Watchdog is a 16 bit programmable down counter. The resolution of the watchdog and wakeup timer is programmable (with prescaler TICK_DV) from approximately 300 μ s to approximately 80ms. By default the resolution is 1ms. The wakeup timer can be started and stopped by user software. The watchdog is disabled after a reset, but if activated it cannot be disabled again, except by another reset. An RTC Wakeup timer timeout also provides a programmable pulse (GTIMER) that can be an output on a GPIO pin.

The GPIO wakeup function lets the software enable wakeup on one or more pins from the P0 GPIO port. The edge sensitivity (rising, falling or both) and de-bouncing filter is individually programmable for each pin.

1.7 XTAL Oscillator

The microcontroller, AD converter and transceiver run on the same crystal oscillator generated clock. A range of crystals frequencies from 4 to 20 MHz may be utilized. For details, please see chapter 7.1 on page 17. The oscillator may be started and stopped as requested by software.



1.8 AD Converter

The nRF9E5 AD converter has up to 10-bit dynamic range and linearity with a conversion rate of 80 ksps used at the Nyquist rate. The reference for the AD converter is software selectable between the AREF input and an internal 1.22V bandgap reference. The converter has 5 inputs selectable by software. Selecting one of the inputs 0 to 3 will convert the voltage on the respective AIN0 to AIN3 pin. Input 4 enables software to monitor the nRF9E5 supply voltage by converting an internal input that is $V_{DD}/3$ with the 1.22V internal reference selected. The AD converter is typically used in a start/stop mode. The sampling time is then under software control. The converter is by default configured as 10 bits. For special requirements, the AD converter can be configured by software to perform 6, 8 or 12 bit conversions. The converter may also be used in differential mode with AIN0 used as negative input and one of the other 3 external inputs used as noninverting input.

1.9 Radio Transceiver

The transceiver part of the circuit has identical functionality to the nRF905 single chip RF transceiver. It is accessed through an internal parallel port and / or an internal SPI. The data ready, carrier-detect and address match signals can be programmed as interrupts to the microcontroller or polled via a GPIO port.

The nRF905 is a radio transceiver for the 433/868/915 MHz ISM bands. The transceiver consists of a fully integrated frequency synthesizer, a power amplifier, a modulator and a receiver unit. Output power and frequency channels and other RF parameters are easily programmable by use of the on chip SPI interface to the nRF905 core. RF current consumption is only 11 mA in TX mode (output power -10dBm) and 12.5 mA in RX mode. For power saving the transceiver can be turned on / off under software control.



2 ELECTRICAL SPECIFICATION

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
Operating conditions						
VDD	Supply voltage		1.9	3.0	3.6	V
TEMP	Operating temperature		-40	27	85	°C
Digital input pin						
V _{IH}	HIGH level input voltage		VDD-0.3		VDD	V
V _{IL}	LOW level input voltage		VSS		0.3	V
Digital output pin						
V _{OH}	HIGH level input voltage (I _{OH} =-0.5mA)		VDD-0.3		VDD	V
V _{OL}	LOW level input voltage (I _{OL} =0.5mA)		VSS		0.3	V
General electrical specification						
I _{PD}	Supply current in power down mode			2.5		µA
General microcontroller conditions						
I _{VDD MCU}	Supply current @4MHz @3V			1		mA
I _{OL_HD}	High drive sink current for P06, P04, P02 and P00 @ V _{OL} = 0.4V	1)			10	mA
I _{OH_HD}	High drive source current for P07, P05, P03 and P01 @ V _{OH} = VDD-0.4V	1)			10	mA
f _{LP OSC}	Low power RC oscillator frequency		1		5.5	KHz
General RF conditions						
f _{OP}	Operating frequency	2)	430		928	MHz
f _{XTAL}	Crystal frequency	3)	4		20	MHz
Δf	Frequency deviation		±42	±50	±58	kHz
R _{GFSK}	GFSK data rate, Manchester-encoded			100		kbps
f _{CH 433}	Channel spacing @ 433MHz			100		kHz
f _{CH 868}	Channel spacing @ 868 and 915 MHz			200		kHz
Transmitter operation						
P _{RF10}	Output power 10dBm setting	4)	7	10	11	dBm
P _{RF6}	Output power 6dBm setting	4)	3	6	9	dBm
P _{RF-2}	Output power -2dBm setting	4)	-6	-2	2	dBm
P _{RF-10}	Output power -10dBm setting	4)	-14	-10	-6	dBm
P _{BW}	20dB bandwidth for modulated carrier			190		kHz
P _{RF1}	1 st adjacent channel transmit power	5)		-27		dBc
P _{RF2}	2 nd adjacent channel transmit power	5)		-54		dBc
I _{TX10dBm}	Supply current @ 10dBm output power			30		mA
I _{TX-14dBm}	Supply current @ -10dBm output power			11		mA
Receiver operation						
I _{RX}	Supply current in receive mode			12.5		mA
RX _{SENS}	Sensitivity at 0.1%BER			-100		dBm
RX _{MAX}	Maximum received signal		0			dBm
C/I _{CO}	C/I Co-channel	6)		13		dB
C/I _{1ST}	1 st adjacent channel selectivity C/I 200kHz	6)		-7		dB
C/I _{2ND}	2 nd adjacent channel selectivity C/I 400kHz	6)		-16		dB
C/I _{IM}	Image rejection	6)		-30		dB

Table 4 nRF9E5 electrical specification.



Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
ADC operation						
DNL	Differential Nonlinearity $f_{IN} = 0.9991$ kHz			± 0.5		LSB
INL	Integral Nonlinearity $f_{IN} = 0.9991$ kHz			± 0.75		LSB
SNR	Signal to Noise Ratio (DC input)			59		dBFS
V_{OS}	Midscale offset			± 1		%FS
ϵ_G	Gain Error			± 1		%FS
SNR	Signal to Noise Ratio (without harmonics) $f_{IN} = 10$ kHz		53	58		dBFS
SFDR	Spurious Free Dynamic Range $f_{IN} = 10$ kHz			65		dB
V_{BG}	Internal reference		1.1	1.22	1.3	V
	Internal reference voltage drift			100		ppm/°C
V_{FS}	Reference voltage input (external ref)		0.8		1.5	V
f_S	Conversion rate	7)			125	ksps
I_{ADC}	Supply current ADC operation			1		mA
t_{NPD}	Start-up time from ADC Power down			15		μs

Table 5 nRF9E5 AD converter electrical specifications.

- 1) Higher sink/source current is possible if increased voltage changes on ports are accepted.
- 2) Operates in the 433, 868 and 915 MHz ISM band.
- 3) The crystal frequency may be chosen from 5 different values (4, 8, 12, 16, and 20MHz) which are specified in the configuration word. Please see Table 22 on page 36.
- 4) De-embedded Antenna load impedance = 400 Ω .
- 5) Channel width and channel spacing is 200kHz.
- 6) Channel Level +3dB over sensitivity, interfering signal a standard carrier wave.
- 7) Conversion rate is dependant on resolution, Please see chapter 10.3 page 30.

2.1 Detailed Current Information

MODE	TYPICAL CURRENT
Light power down	0.4 mA
Moderate Power down	125 μA
Standby mode	25 μA
Deep Power Down	2.5 μA
MCU @0.5M 3 volt	0.125 mA
MCU @1M 3 volt	0.25 mA
MCU @2M 3 volt	0.5 mA
MCU @4M 3 volt	1 mA
MCU @8M 3 volt	2 mA
MCU @12M 3 volt	3 mA
MCU @16M 3 volt	4 mA
MCU @20M 3 volt	5 mA
Rx @ 433	12.2 mA
Rx @ 868/915	12.8 mA
Reduced Rx	10.5 mA
Tx @ 10dBm	30 mA
Tx @ 6dBm	20 mA
Tx @ -2dBm	14 mA
Tx @ -10dBm	11 mA

Table 6 Detailed current information



3 PIN ASSIGNMENT

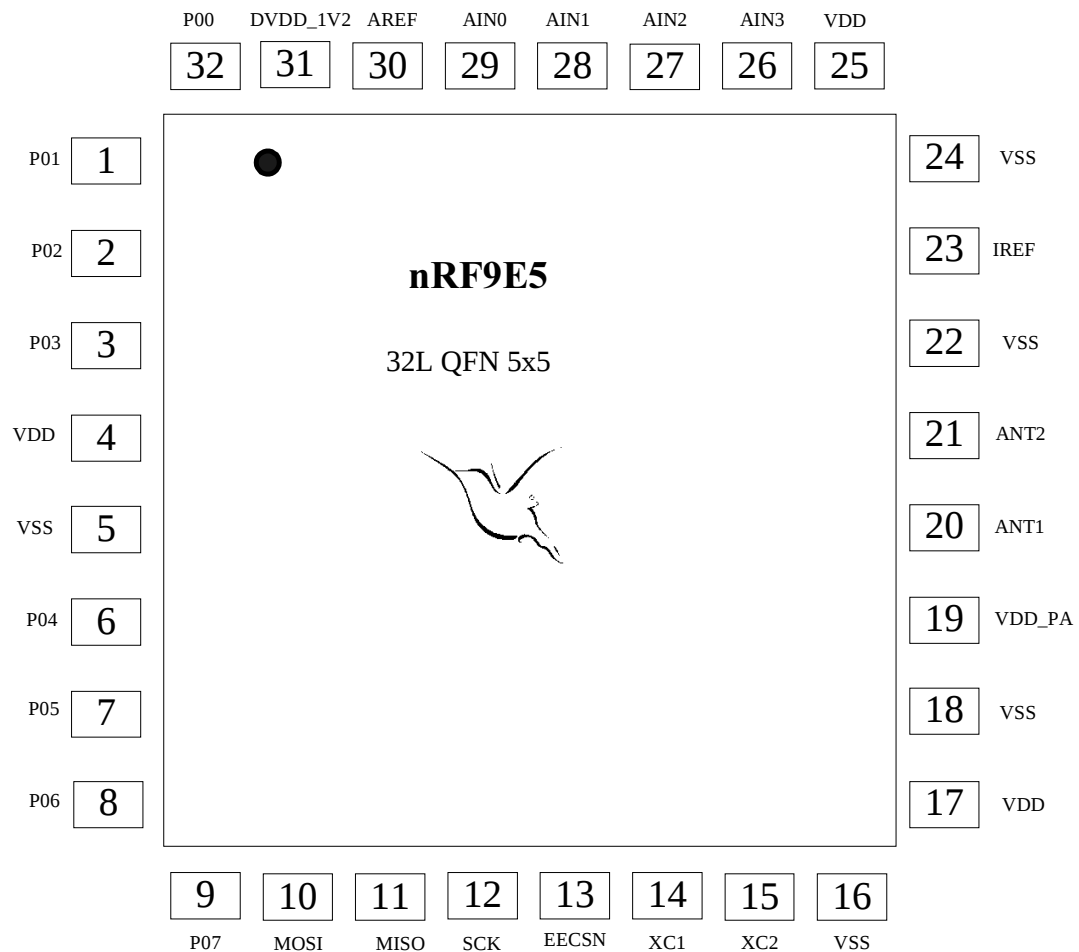


Figure 2 Pin assignment nRF9E5.



4 PIN FUNCTION

Pin	Name	Pin function	Description
1	P01	Digital IN/OUT	uP Bi-directional digital pin
2	P02	Digital IN/OUT	uP Bi-directional digital pin
3	P03	Digital IN/OUT	uP Bi-directional digital pin
4	VDD	Power	Power supply (+3V DC)
5	VSS	Power	Ground (0V)
6	P04	Digital IN/OUT	uP Bi-directional digital pin
7	P05	Digital IN/OUT	uP Bi-directional digital pin
8	P06	Digital IN/OUT	uP Bi-directional digital pin
9	P07	Digital IN/OUT	uP Bi-directional digital pin
10	MOSI	SPI-Interface	SPI output
11	MISO	SPI-Interface	SPI input
12	SCK	SPI-clock	SPI clock
13	EECSN	SPI-enable	SPI enable, active low
14	XC1	Analog Input	Crystal Pin 1/ External clock reference pin
15	XC2	Analog Output	Crystal Pin 2
16	VSS	Power	Ground (0V)
17	VDD	Power	Power supply (+3V DC)
18	VSS	Power	Ground (0V)
19	VDD_PA	Power Output	Regulated positive supply (1.8V) to nRF905 power amplifier
20	ANT1	RF – port	Antenna interface 1
21	ANT2	RF – port	Antenna interface 2
22	VSS	Power	Ground (0V)
23	IREF	Analog Input	Reference current
24	VSS	Power	Ground (0V)
25	VDD	Power	Power supply (+3V DC)
26	AIN3	Analog Input	ADC Input 3
27	AIN2	Analog Input	ADC Input 2
28	AIN1	Analog Input	ADC Input 1
29	AIN0	Analog Input	ADC Input 0
30	AREF	Analog Input	ADC Reference Voltage
31	DVDD_1V2	Power Output	Low voltage positive digital supply output for de-coupling
32	P00	Digital IN/OUT	uP Bi-directional digital pin

Table 7 nRF9E5 pin function.



5 SYSTEM CLOCK

The Microcontroller clock, CPU_CLK, is generated from the on chip crystal oscillator. CPU_CLK frequency is configured in the RF-configuration register (see chapter 11) and could be set to 0.5, 1, 2 or 4MHz. CPU_CLK could in addition be set equal to the crystal oscillator frequency itself. The CPU_CLK generation is illustrated in Figure 3.

It is important to always set XOF equal to the actual crystal selected for the application.

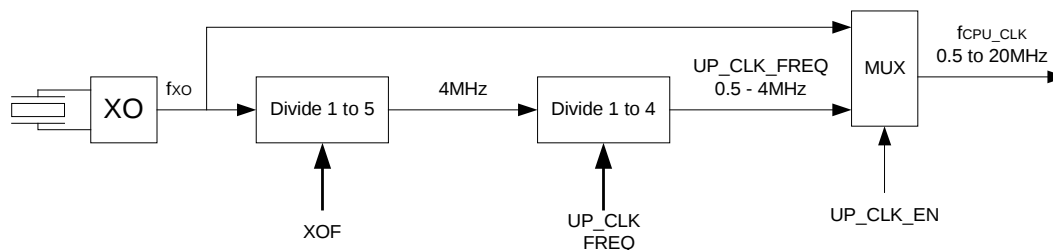


Figure 3 CPU_CLK generation in nRF9E5.

The chip has an internal low frequency clock that is always active. This clock ensure proper operation of vital function when the chip is in power down mode and the crystal oscillator is turned off, please see chapter 16 on page 50.



6 DIGITAL I/O PORTS

The nRF9E5 has two IO ports located at the default locations for P0 and P1 in standard 8051, but the ports are fully bi-directional CMOS and the direction of each pin is controlled by a `_DIR` and an `_ALT` bit for each bit as shown in the table below.

Pin	Default function	Alternate=1	SPI_CTRL != 01
EECSN	P1.3		P1.3
MISO	SPI.datain		P1.2
SCK	SPI.clock	T2 (timer2 input)	P1.0
MOSI	SPI.dataout		P1.1
P00	P0.0	GTIMER	
P01	P0.1	RXD (UART)	
P02	P0.2	TXD (UART)	
P03	P0.3	INT0_N (interrupt)	
P04	P0.4	INT1_N (interrupt)	
P05	P0.5	T0 (timer0 input)	
P06	P0.6	T1 (timer1 input)	
P07	P0.7	PWM	

Table 8 Port functions.

6.1 I/O Port Behavior During RESET

During this period the internal reset is active (regardless of whether or not the clock is running), all the port pins related to P0 are configured as inputs, whereas the inputs related to P1 are configured as required for an SPI master. When program execution starts, all ports are still configured as during reset, and the program will need to set the `_ALT` and/or the `_DIR` register for the pins that need another direction.

6.2 Port 0 (P0)

P0_ALT and P0_DIR control the P0 port function in that order of priority. If the alternate function for port P0.n is set (by P0_ALT.n = 1) the pin will be input or output as required by the alternate function (UART, external interrupt, timer inputs or PWM output), except that the UART RXD direction will still depend on P0_DIR.1.

To use INT0_N or INT1_N as interrupts, the corresponding alternate function must be activated, P0_ALT.3 / P0_ALT.4. When the P0_ALT.n is not set, bit 'n' of the port is a GPIO function with the direction controlled by P0_DIR.n.

Pin	Data in P0_ALT.n,P0_DIR.n							
	10		11		00		01	
P00	GTIMER	Out	GTIMER	Out	P0.0	Out	P0.0	In
P01	RXD	Out	RXD	In	P0.1	Out	P0.1	In
P02	TXD	Out	TXD	Out	P0.2	Out	P0.2	In
P03	INT0_N	In	INT0_N	In	P0.3	Out	P0.3	In
P04	INT1_N	In	INT1_N	In	P0.4	Out	P0.4	In
P05	T0	In	T0	In	P0.5	Out	P0.5	In
P06	T1	In	T1	In	P0.6	Out	P0.6	In
P07	PWM	Out	PWM	Out	P0.7	Out	P0.7	In

Table 9 Port 0 (P0) functions.



Port 0 is controlled by SFR-registers 0x80, 0x93, 0x94 and 0x95 listed in the table below.

Addr SFR (hex)	R/W	#bit	Init value (hex)	Name	Function
80	R/W	8	FF	P0	Port 0, pins P07 to P00
93	R/W	8	00	P0_DRV	High drive strength for each bit of Port 0 0: Enable, 1: Disable (See 6.2.1 below for a description)
94	R/W	8	FF	P0_DIR	Direction for each bit of Port 0 0: Output, 1: Input Direction is overridden if alternate function is selected for a pin.
95	R/W	8	00	P0_ALT	Select alternate functions for each pin of P0, if corresponding bit in P0_ALT is set, as listed in Table 9 Port 0 (P0) functions.

Table 10 Port 0 control and data SFR-registers.

6.2.1 High Current Drive Capability

Odd numbered bits will source high current when the corresponding bit in P0_DRV is set, where as even number bits will sink high current when the corresponding bit in P0_DRV is set.

6.3 Port 1 (P1 or SPI port)

The P1 port consists of 4 pins, one of which is a hardwired input. The primary function of the P1 port (when SPI_CTRL is 01) is a SPI master port. The pin EECSN is used as a chip select for the boot EEPROM, the GPIO bits in port P0 may be used as chip select(s) for other SPI devices.

When not used as SPI port, P1_ALT.0 will force SCK (P1.0) to be the timer T2 input; MOSI (P1.1) is now a GPIO. When P0_ALT.0 is 0, also SCK (P1.0) is a GPIO.

MISO (P1.2) is always an input. That is P1_DIR.2 and P1_ALT.2 are ignored.

EECSN (P1.3) is always a GPIO. It will be activated by the default boot loader after reset and should be connected to the CSN of the boot flash.

Pin	SPI_CTRL = 01		SPI_CTRL != 01					
			P1_ALT.n = 1		P1_ALT.n = 0			
					P1_DIR.n = 0		P1_DIR.n = 1	
SCK	SPI.clock	Out	T2	In	P1.0	In	P1.0	Out
MOSI	SPI.dataout	Out	P1.1	I/O ²	P1.1	In	P1.1	Out
MISO	SPI.datain	In	P1.2	In	P1.2	In	P1.2	In
EECSN	P1.3	Out	P1.3	I/O ²	P1.3	In	P1.3	Out

Table 11 Port 1 (P1) functions.

² P1.1 and P1.3 are actually under control of P1_DIR.1 and P1_DIR.3 even when P1_ALT.1 or P1_ALT.3 are 1, since there are no alternate functions for these pins.



Port 1 is controlled by SFR-registers 0x90, 0x96 and 0x97, and only the 4 lower bits of the registers are used.

Addr SFR (hex)	R/W	#bit	Init value (hex)	Name	Function
90	R/W	4	F	P1	Port 1, pins SPI_SCK, SPI_MOSI, SPI_MISO and SPI_CSN
96	R/W	4	4	P1_DIR	Direction for each bit of Port 1 0: Output, 1: Input Direction is overridden if alternate function is selected for a pin, or if SPI_CTRL=01. SPI_MISO is always input.
97	R/W	4	0	P1_ALT	Select alternate functions for each pin of P1 if corresponding bit in P1_ALT is set, as listed in Table 11 Port 1 (P1) functions

Table 12 Port 1 control and data SFR-registers.

P1 is by default configured as a SPI master port. In this case, it is then controlled by the 3 SFR registers 0xB2, 0xB3 and 0xB4 as shown in Table 33 on page 42.



7 ANALOG INTERFACE

7.1 Crystal Specification

Tolerance includes initially accuracy and tolerance over temperature and aging.

Frequency	C _L	ESR	C _{0max}	Tolerance @ 868/915 MHz	Tolerance @ 433 MHz
4MHz	12pF	150Ω	7.0pF	±30ppm	±60ppm
8MHz	12pF	100Ω	7.0pF	±30ppm	±60ppm
12MHz	12pF	100Ω	7.0pF	±30ppm	±60ppm
16MHz	12pF	100Ω	7.0pF	±30ppm	±60ppm
20MHz	12pF	100Ω	7.0pF	±30ppm	±60ppm

Table 13 Crystal specification of nRF9E5.

To achieve a crystal oscillator solution with low power consumption and fast start-up time, it is recommended to specify the crystal with a low value of crystal load capacitance. Specifying C_L =12pF is acceptable, but it is possible to use up to 16pF. Specifying a lower value of crystal parallel equivalent capacitance, Co=1.5pF is also good, but this can increase the price of the crystal itself. Typically Co=1.5pF at a crystal specified for Co_{max}=7.0pF.

7.2 Antenna Output

The “ANT1 & ANT2” output pins provide a balanced RF output to the antenna. The pins must have a DC path to VDD_PA, either via a RF choke or via the center point in a dipole antenna. The load impedance seen between the ANT1/ANT2 outputs should be in the range 200-700Ω. A low load impedance (for instance 50Ω) can be obtained by fitting a simple matching network or a RF transformer (balun). Further information regarding balun structures and matching networks may be found in the Application Examples chapter.

7.3 ADC Inputs

The Analog to digital converter has four analog input channels and one reference voltage input. Analog input is selected with CHSEL in the ADC_CONFIG_REG.

7.4 Current Reference

To get accurate internal biasing, an external low tolerance resistor is used. A resistor of 22kΩ and 1% accuracy should be connected between the pin IREF and ground for proper operation of nRF9E5.

7.5 Digital Power De-Coupling

nRF9E5 has internal regulator used for optimum performance and minimum power dissipation in digital part of the system. De-coupling of the regulated power is needed for proper operation of the chip. A capacitor of 10nF should be connected between DVDD_1V2 and ground as close to the chip as possible. Please see PCB layout and de-coupling guidelines for further information regarding layout.



8 INTERNAL INTERFACE AD CONVERTER AND TRANSCEIVER

8.1 P2 - Radio General Purpose IO Port

The P2 port controls the transceiver. The P2 port uses the address normally used by port P2 in standard 8051. However since the radio transceiver is on chip, the port is not bi-directional. The power on default values in the port “latch” also differs from traditional 8051 to match the requirements of the radio transceiver subsystem.

Operation of the transceiver is controlled by SFR registers P2 and SPI_CTRL:

Addr SFR (hex)	R/W	#bit	Init value (hex)	Name	Function
A0	R/W	8	04	P2	General purpose IO for interface to nRF905 radio transceiver and AD converter subsystems
B3	R/W	2	0	SPI_CTRL	00 -> SPI not used 01 -> SPI connected to port P1 (boot) 1x -> SPI connected to nRF905/AD

Table 14 nRF905 433/868/915 MHz transceiver subsystem control registers - SFR 0xA0 and 0xB3.

The bits of the P2 register correspond to similar pins of the nRF905 single chip, as shown in Table 15 P2 (RADIO) register . In the documentation the pin names are used, so please note that setting or reading any of these nRF905 pins, means to write or read the P2 SFR register accordingly.

P2 register bit: Function	Corresponding nRF905 Transceiver pin name
Read :	
7: nRF905 Transceiver address match	AM
6: nRF905 Transceiver carrier detect	CD
5: nRF905 Transceiver data ready	DR
4: ADC end of conversion	EOC
3: 0 (not used)	
2: nRF905 Transceiver and ADC SPI data out (SBMISO)	MISO
1: 0 (not used)	
0: 0 (not used)	
Write :	
7: Not used	
6: Not used	
5: nRF905 Transceiver enable receiver function	TRX_CE
4: nRF905 Transceiver transmit/receive selection	TX_EN
3: nRF905 Transceiver and ADC SPI Chip select (SBCSN)	CSN
2: Not used	
1: nRF905 Transceiver and ADC SPI data in (SBMOSI)	MOSI
0: nRF905 Transceiver and ADC SPI clock (SBCK)	SCK

Table 15 P2 (RADIO) register - SFR 0xA0, default initial data value is 0x08.

Note : Some of the pins are overridden when SPI_CTRL=1x, see Table 14.



8.1.1 Controlling the Transceiver via SPI Interface.

Normally the SPI hardware interface rather than GPIO programming will do the data transfers to the transceiver. Please see Table 33 SPI control and data SFR-registers for use of SPI interface. When SPI_CTRL is '0x', all radio pins are connected directly to their respective port pins and the SPI functionality may be implemented in software.

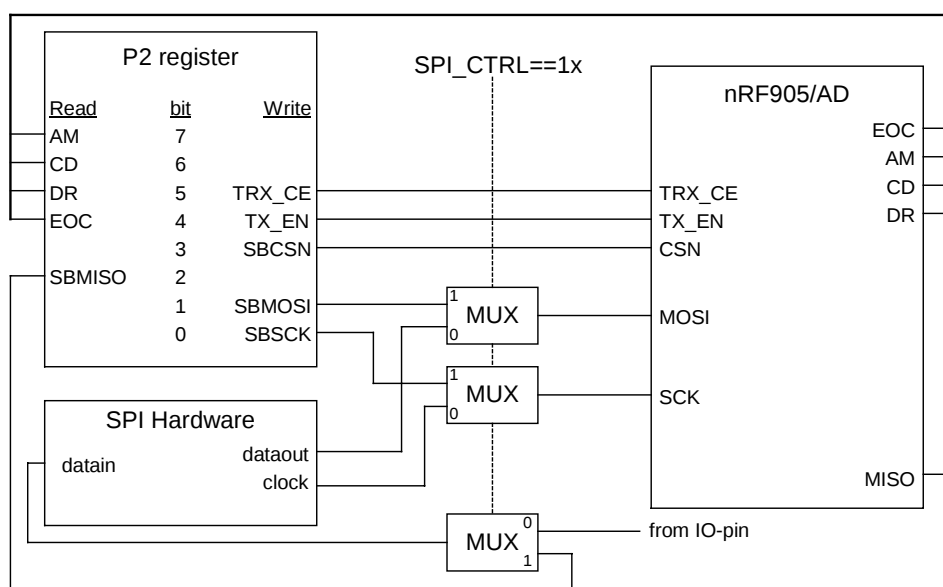


Figure 4 Transceiver interface.

8.1.2 P2 Port Behavior During RESET

During the period the internal reset is active (regardless of whether or not the clock is running), the P2 outputs that control the nRF905 transceiver subsystem are forced to their respective default values. When program execution starts, these ports will remain at those default levels until the programmer actively changes them by writing to the P2 register.



9 TRANCEIVER SUBSYSTEM (nRF905)

9.1 RF Modes of Operation

The Transceiver has two active (RX/TX) modes and one power-saving mode when the microcontroller is running.

9.1.1 Active Modes

- ShockBurst™ RX
- ShockBurst™ TX

9.1.2 Power Saving Mode

- Standby and SPI - programming

The transceiver mode is decided by the settings of TRX_CE, TX_EN

TRX CE	TX EN	Operating Mode
0	X	Standby and SPI – programming
1	0	Radio Enabled - ShockBurst™ RX
1	1	Radio Enabled - ShockBurst™ TX

Table 16 transceiver operational modes.

9.2 nRF ShockBurst™ Mode

The nRF9E5 uses the Nordic VLSI ShockBurst™ feature. ShockBurst™ makes it possible to use the high data rate offered by the nRF905. By embedding all high speed signal processing related to RF protocol in the transceiver, the nRF905 offers the micro controller a simple SPI interface. Data rate is decided by the interface-speed the micro controller itself sets up. By allowing the digital part of the application to run at low speed, while maximizing the data rate on the RF link, the nRF905 ShockBurst™ mode reduces the average current consumption in applications. In ShockBurst™ RX, Address Match (AM) and Data Ready (DR) notifies the MCU when a valid address and payload is received respectively. In ShockBurst™ TX, the nRF905 automatically generates preamble and CRC. Data Ready (DR) notifies the MCU that the transmission is completed. All together, this means reduced memory demand and more available resources in the MCU, as well as reduced software development time.

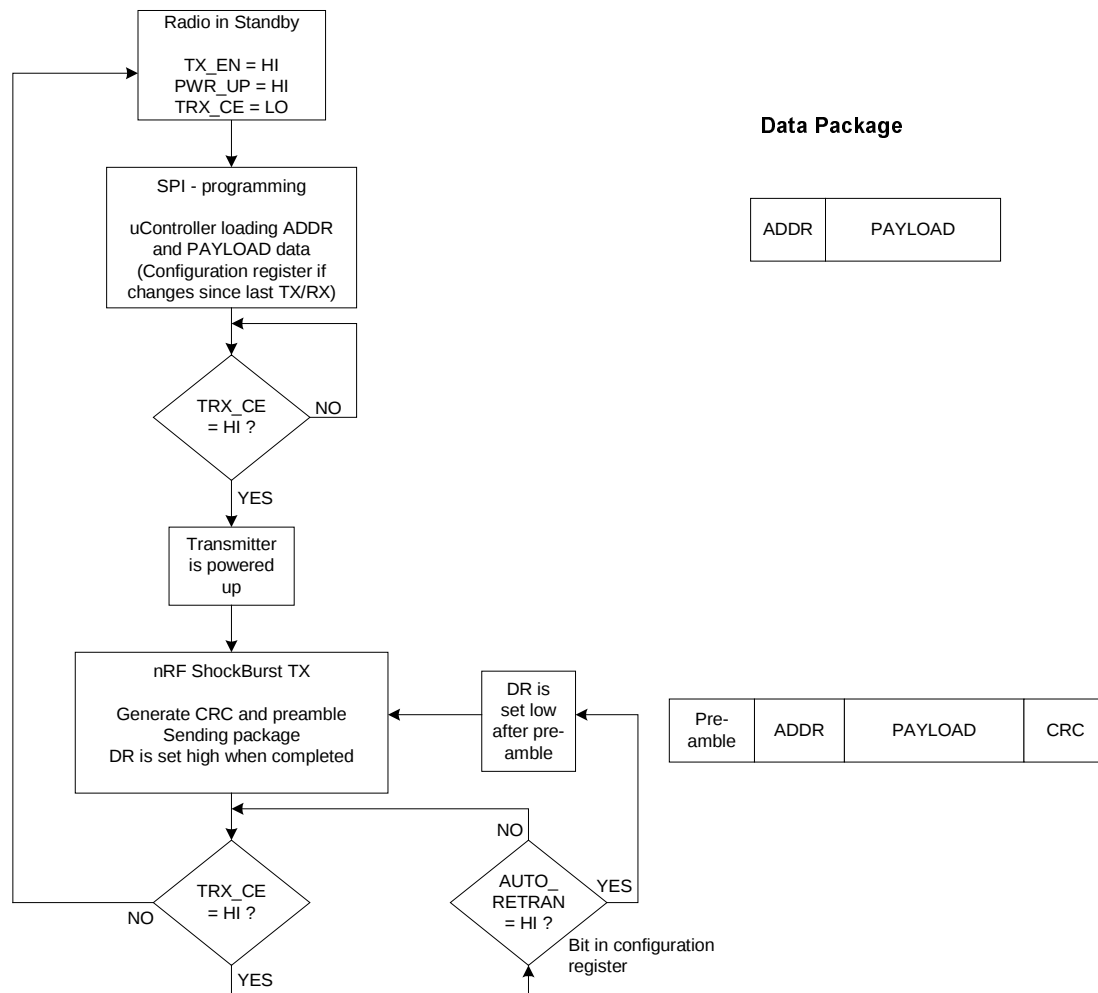


Typical ShockBurst™ TX:

1. When the application MCU has data for a remote node, the address of the receiving node (TX-address) and payload data (TX-payload) are clocked into nRF905 via the SPI interface. The application protocol or MCU sets the speed of the interface.
2. MCU sets TRX_CE and TX_EN high, this activates a nRF905 ShockBurst™ transmission.
3. nRF905 ShockBurst™:
 - Radio is automatically powered up.
 - Data package is completed (preamble added, CRC calculated).
 - Data package is transmitted (100kbps, GFSK, Manchester-encoded).
 - Data Ready is set high when transmission is completed.
4. If AUTO_RETRAN is set high, the nRF905 continuously retransmits the package until TRX_CE is set low.
5. When TRX_CE is set low, the nRF905 finishes transmitting the outgoing package and then sets itself into standby mode.

The ShockBurst™ mode ensures that a transmitted package that has started always finishes regardless of what TRX_EN and TX_EN is set to during transmission. The new mode is activated when the transmission is completed. Please see subsequent chapters for detailed timing

For test purposes such as antenna tuning and measuring output power it is possible to set the transmitter so that a constant carrier is produced. To do this TRX_CE must be maintained high instead of being pulsed. In addition Auto Retransmit should be switched off. After the burst of data has been sent then the device will continue to send the unmodulated carrier.



NB: DR is set low under the following conditions after it has been set high:

- If TX_EN is set low

Figure 5 Flowchart ShockBurst™ transmit of nRF905.



Typical ShockBurst™ RX:

1. ShockBurst™ RX is selected by setting TRX_CE high and TX_EN low.
2. After 650µs nRF905 is monitoring the air for incoming communication.
3. When the nRF905 senses a carrier at the receiving frequency, Carrier Detect (CD) pin is set high.
4. When a valid address is received, Address Match (AM) pin is set high.
5. When a valid package has been received (correct CRC found), nRF905 removes the preamble, address and CRC bits, and the Data Ready (DR) pin is set high.
6. MCU sets the TRX_CE low to enter standby mode (low current mode).
7. MCU can clock out the payload data at a suitable rate via the SPI interface.
8. When all payload data is retrieved, nRF905 sets Data Ready (DR) and Address Match (AM) low again.
9. The chip is now ready for entering ShockBurst™ RX, ShockBurst™ TX or power down mode.

If TRX_CE or TX_EN is changed during an incoming package, the nRF905 changes mode immediately and the package is lost. However, if the MCU is sensing the Address Match (AM) pin, it knows when the chip is receiving an incoming package and can therefore decide wheather to wait for the Data Ready (DR) signal or enter a different mode.

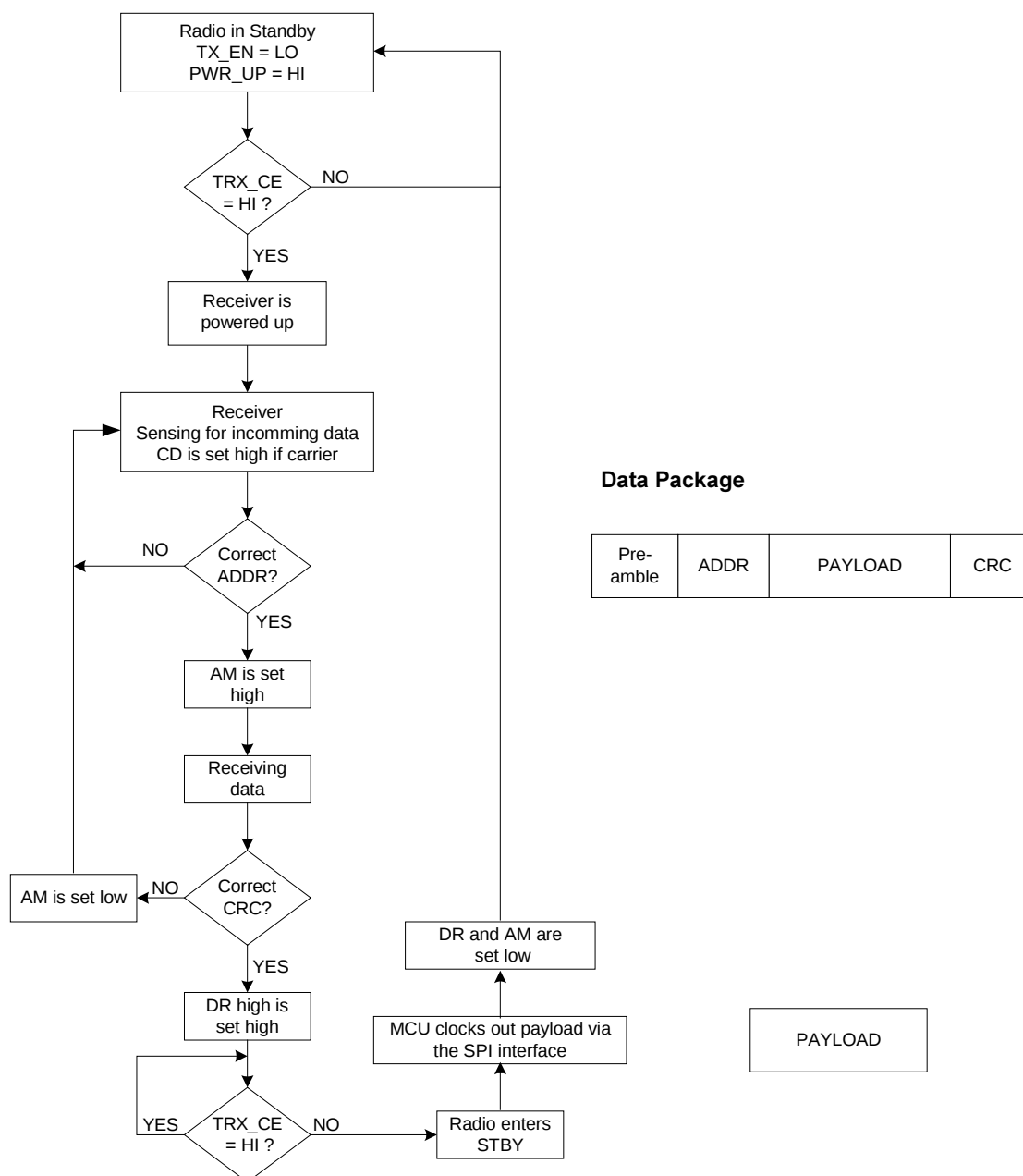


Figure 6 Flowchart ShockBurst™ receive of nRF905.



9.3 Standby Mode

Standby mode is used to minimize average current consumption while not transmitting or receiving and still maintaining short start up times to ShockBurstTM RX and ShockBurstTM TX. In this mode the crystal oscillator have to be active. The configuration word content is maintained during standby.

9.4 Output Power Adjustment

The power amplifier in nRF905 can be programmed to four different output power settings by the configuration register. By reducing output power, the total TX current is reduced.

Power setting	RF output power	DC current consumption
00	-10 dBm	11.0 mA
01	-2 dBm	14.0 mA
10	6 dBm	20.0 mA
11	10 dBm	30.0 mA
Conditions: VDD = 3.0V, VSS = 0V, TA = 27°C, Load impedance = 400 Ω .		

Table 17 RF output power setting for the nRF905.

9.5 Modulation

The modulation of nRF905 is Gaussian Frequency Shift Keying (GFSK) with a data-rate of 100kbps. Deviation is ± 50 kHz. GFSK modulation results in a more bandwidth effective transmission-link compared with ordinary FSK modulation.

The data is internally Manchester encoded (TX) and Manchester decoded (RX). That is, the effective symbol-rate of the link is 50kbps. By using internally Manchester encoding, no scrambling in the u-controller is needed.



9.6 Output Frequency

The operating RF-frequency of nRF905 is set in the configuration register by CH_NO and HFREQ_PLL. The operating frequency is given by:

$$f_{op} = (422.4 + (CH_NO/10)) \cdot (1 + HFREQ_PLL) \text{ MHz}$$

When HFREQ_PLL is '0' the frequency resolution is 100kHz and when it is '1' the resolution is 200kHz.

The application operating frequency has to be chosen to apply with the Short Range Devise regulation in the area of operation.

Operating frequency	HFREQ_PLL	CH_NO
430.0 MHz	[0]	[001001100]
433.1 MHz	[0]	[001101011]
433.2 MHz	[0]	[001101100]
434.7 MHz	[0]	[001111011]
862.0 MHz	[1]	[001010110]
868.2 MHz	[1]	[001110101]
868.4 MHz	[1]	[001110110]
869.8 MHz	[1]	[001111101]
902.2 MHz	[1]	[100011111]
902.4 MHz	[1]	[100100000]
927.8 MHz	[1]	[110011111]

Table 18 Examples of real operating frequencies.

9.7 Carrier Detect.

When the nRF905 is in ShockBurstTM RX, the Carrier Detect (CD) pin is set high if a RF carrier is present at the channel the device is programmed to. This feature is very effective to avoid collision of packages from different transmitters operating at the same frequency. Whenever a device is ready to transmit it could first be set into receive mode and sense whether or not the wanted channel is available for outgoing data. This forms a very simple listen before transmit protocol. Operating Carrier Detect (CD) with Reduced RX Power mode is an extremely power efficient RF system. Typical Carrier Detect level (CD) is typically 5dB lower than sensitivity, i.e. if sensitivity is -100dBm then the Carrier Detect function will sense a carrier wave as low as -105dBm. Below -105dBm the Carrier Detect signal will be low, i.e. 0V. Above -95dBm the Carrier Detect signal will be high, i.e. Vdd. Between -105 to 106 the Carrier Detect Signal will toggle.



9.8 Address Match

When the nRF905 is in ShockBurst™ RX mode, the Address Match (AM) pin is set high as soon as an incoming package with an address that is identical with the device's own identity is received. With the Address Match pin the controller is alerted that the nRF905 is receiving data actually before the Data Ready (DR) signal is set high. If the Data Ready (DR) pin is not set high i.e. the CRC is incorrect then the Address Match (AM) pin is reset to low at the end of the received data packet. This function can be very useful for an MCU. If Address Match (AM) is high then the MCU can make a decision to wait and see if Data Ready (DR) will be set high indicating a valid data package has been received or ignore that a possible package is being received and switch modes.

9.9 Data Ready

The Data Ready (DR) signal makes it possible to largely reduce the complexity of the MCU software program.

In ShockBurst™ TX, the Data Ready (DR) signal is set high when a complete package is transmitted, telling the MCU that the nRF905 is ready for new actions. It is reset to low at the start of a new package transmission or when switched to a different mode i.e. receive mode or standby mode.

In ShockBurst™ TX Auto Retransmit the Data Ready (DR) signal is set high at the beginning of the pre-amble and is set low at the end of the preamble. The Data Ready (DR) signal therefore pulses at the beginning of each transmitted data packet.

In ShockBurst™ RX, the signal is set high when nRF905 has received a valid package, i.e. a valid address, package length and correct CRC. The MCU can then retrieve the payload via the SPI interface. The Data Ready (DR) pin is reset to low once the data has been clocked out of the data buffer or the device is switched to transmit mode.

9.10 Auto Retransmit

One way to increase system reliability in a noisy environment or in a system without collision control is to transmit a package several times. This is easily accomplished with the Auto Retransmit feature in nRF905. By setting the AUTO_RETRAN bit to "1" in the configuration register, the circuit keeps sending the same data package as long as TRX_CE and TX_EN is high. As soon as TRX_CE is set low the device will finish sending the packet it is currently transmitting and then return to standby mode.

9.11 RX Reduced Power Mode

To maximize battery lifetime in application where the nRF905 high sensitivity is not necessary; nRF905 offers a built in reduced power mode. In this mode, the receive current consumption reduces from 12.5mA to only 10.5mA. The sensitivity is reduced to typical -85dBm, ±10dB. Some degradation of the nRF905 blocking performance should be expected in this mode. The reduced power mode is an excellent option when using Carrier Detect to sense if the wanted channel is available for outgoing data.



10 AD CONVERTER SUBSYSTEM

10.1 AD Converter

The nRFE5 AD converter has 10 bit dynamic range and linearity when used at the Nyquist rate. With lower signal frequencies and post filtering, up to 12 bits resolution is possible. The reference for the AD converter is selectable between the AREF input and an internal 1.22V bandgap reference.

The converter default SPI setting is 10 bits. For special requirements, the AD converter can be configured to perform 6, 8, 10 or 12 bit conversions. The converter may also be used in differential mode with AIN0 used as inverting input and one of the other 3 external inputs used as noninverting input.

Two registers interface the AD converter, ADC_CONFIG_REG and ADC_DATA_REG. AD converter status bit are available in the STATUS_REGISTER. Registers are described in detail in chapter 11.

Selection of input channel is directly embedded in the START_ADC_CONV command, alternatively it is set by CHSEL in the ADC_CONFIG_REG. Values of CHSEL from 0 to 3 would select AIN0 to AIN3 respectively. Setting CHSEL to [1xxx] will monitor the nRF9E5 supply voltage by converting an internal input that is VDD/3 with the 1.22V internal reference.

The AD conversion result is available as ADCDATA in ADC_DATA_REG at the end of conversion. The data in ADC_DATA_REG is stored according to Table 19 with left or right justified data selected by ADC_RL_JUST.

ADC_RL_JUST	ADC_RESCTRL	# bit	ADC_DATA_REG[15:0]					
			High byte [15:8]			Low byte [7:0]		
0	00	6	ADCDATA[5:0]					
0	01	8	ADCDATA[7:0]					'0'
0	10	10	ADCDATA[9:0]					
0	11	12	ADCDATA[11:0]					
1	00	6				ADCDATA[5:0]		
1	01	8		'0'		ADCDATA[7:0]		
1	10	10				ADCDATA[9:0]		
1	11	12				ADCDATA[11:0]		

Table 19 ADC_DATA_REGISTER justified data.

Overflow status is stored as ADC_RFLAG in the STATUS_REGISTER after each conversion.

The complete subsystem is switched off by clearing bit ADC_PWR_UP.

Instructions for the AD converter are given in Table 21 on page 34.



10.2 AD Converter Usage

10.2.1 Measurements with External Reference

When VFSSEL is set to 1 and CHSEL selects an input AINi (i.e. AIN0 to AIN3), the result in ADCDATA is directly proportional to the ratio between the voltage on the selected input, and the voltage on pin AREF:

$$V_{AINi} = V_{AREF} \cdot \frac{ADCDATA}{2^N}$$

and for differential measurements a similar equation apply:

$$V_{AINi} - V_{AIN0} = V_{AREF} \cdot \frac{ADCDATA - 2^{(N-1)}}{2^N}$$

Where N is the number of bits set in RESCTRL

This mode of operation is normally selected for sources where the voltage is depending on the supply voltage (or another variable voltage), as shown in Figure 7 below. The resistor R1 is selected to keep $AREF \leq 1.5V$ for the maximum VDD voltage.

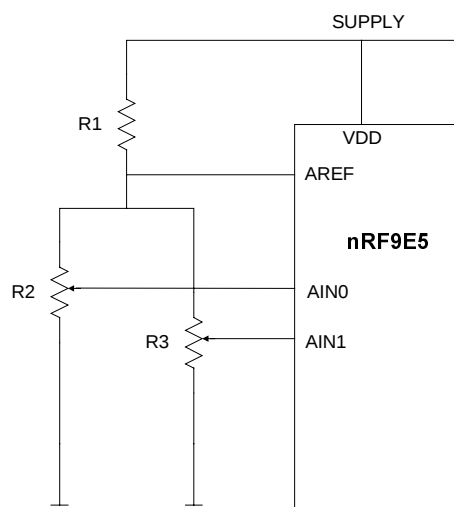


Figure 7 Typical use of AD with 2 ratiometric inputs.



10.2.2 Measurements with Internal Reference

When VFSSEL is set to 0 and CHSEL selects an input AINI (i.e. AIN0 to AIN3), the result in ADCDATA is directly proportional to the ratio between the voltage on the selected input and the internal bandgap reference (nominally 1.22V):

$$V_{AINi} = 1.22 \cdot \frac{ADCDATA}{2^N}$$

and for differential measurements a similar equation apply:

$$V_{AINi} - V_{AIN0} = 1.22 \cdot \frac{ADCDATA - 2^{(N-1)}}{2^N}$$

Where N is the number of bits set in RESCTRL

This mode of operation is normally selected for sources where the voltage is not depending on the supply voltage.

10.2.3 Supply Voltage Measurement

When CHSEL is set to [1xxx], the ADC will use the internal bandgap reference (nominally 1.22V). The input to the converter is 1/3 of the voltage on the VDD pins. The result in ADCDATA is thus directly proportional to the VDD voltage.

$$V_{VDD} = 3.66 \cdot \frac{ADCDATA}{2^N}$$

Where N is the number of bits set in RESCTRL

10.3 AD Converter Sampling and Timing

An AD conversion is initialized after a low to high transition on CSTASRT in ADC_CONFIG_REG or by using the instruction START_ADC_CONV. In both cases the conversion itself would start at the first positive edge of ADCCLK after SBCSN is set high after instruction is issued.

When ADCRUN is low, a single conversion would be performed and a pulse on EOC is generated when the converted value is available in ADC_DATA_REG. If CSTARTN is set low or a new START_ADC_CONV command is issued, the previous conversion will be aborted. Conversion time, t_{conv} , depends on resolution.

$$t_{conv} = \frac{N}{2} + 3 \quad \text{ADCCLK cycles}$$

Where N is the number of resolution bit. In Figure 8 a 10-bit conversion is shown.

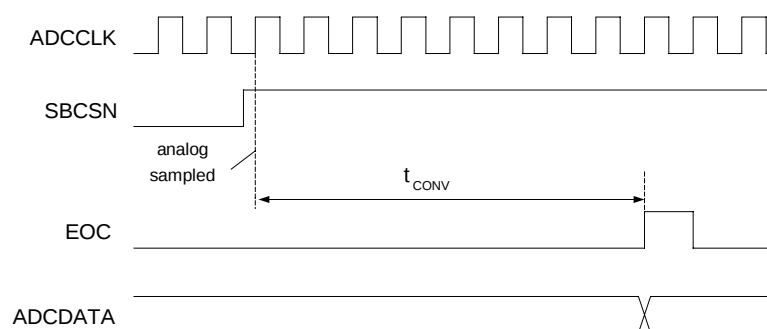


Figure 8 Timing diagram single step conversion.

When ADCRUN is high the ADC is running continuously. Cycle time t_{cycle} is the time between each conversion. EOC indicates every time a new conversion value is stored in ADC_DATA_REG.

$$t_{\text{cycle}} = \frac{N}{2} + 1 \quad \text{ADCCLK cycles}$$

where N is number of resolution bits. Figure 9 shows 10-bit conversion where ADCRUN is set high.

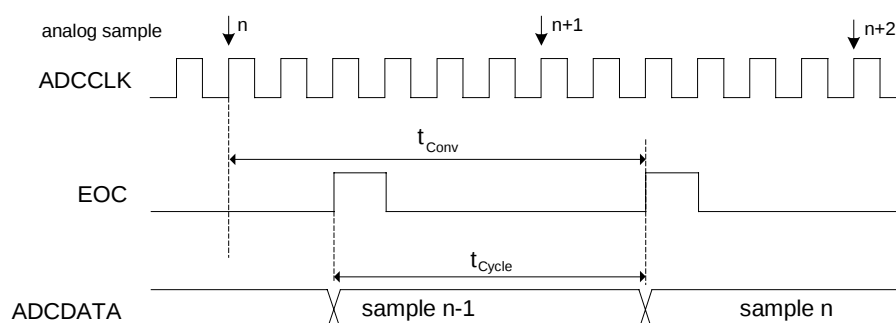


Figure 9 Timing diagram continuous mode conversion.

A 500 kHz clock (ADCCLK) clocks the ADC converter. Table 20 shows t_{cycles} as function of resolution.

Resolution [Number of bits]	t_{cycles} [μs]	Sampling rate [ksps]
6	8	125
8	10	100
10	12	83.3
12	14	71.4

Table 20 ADC resolution and maximum sampling rate.



11 TRANCEIVER AND AD CONVERTER CONFIGURATION

All configuration of the transceiver and AD converter subsystem is done via an internal SPI-interface of the two systems. The interface consists of 7 registers, a SPI instructions set is used to decide which operation shall be performed. The SPI-interface can only be activated when the transceiver is in standby mode. All references to the SPI interface in this chapter refer to the internal SPI interface of the transceiver and AD converter subsystem.

11.1 Internal SPI Register Configuration

The SPI-interface consists of seven internal registers. A register read-back mode is implemented to allow verification of the register contents

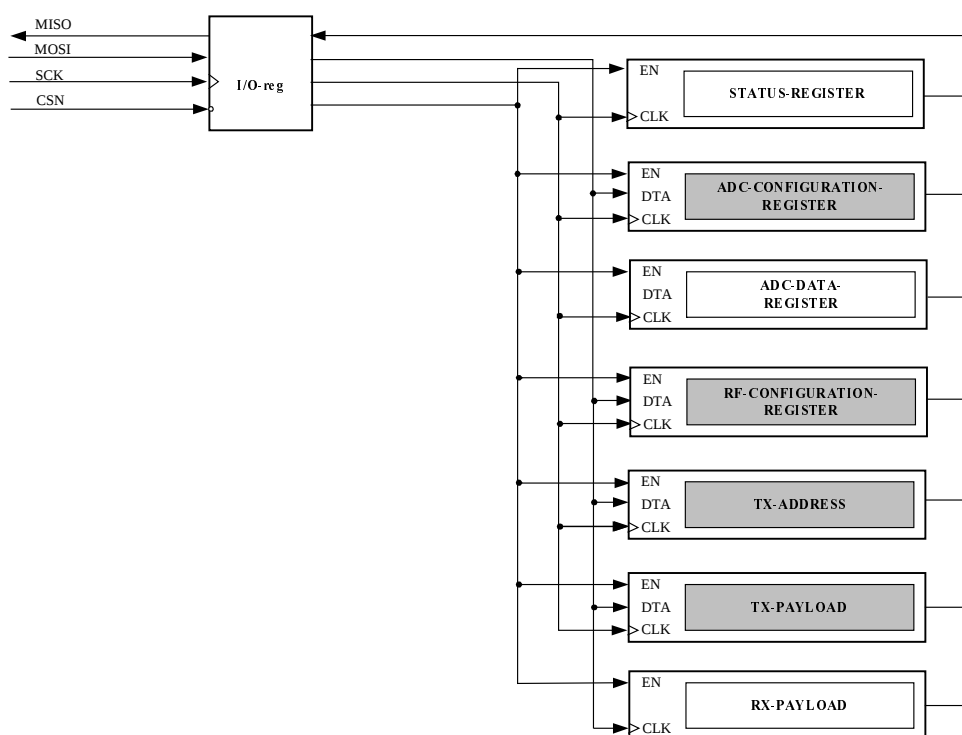


Figure 10 SPI – interface composed of seven internal registers.

Status – Register

Register contains status of Data Ready (DR), Address Match (AM), ADC_End_Of_Conversion and ADC_Ready_Flag

ADC- Configuration – Register

Register contains information of ADC setup such as resolution control, channel select, differential or single ended mode, continuous or single conversion mode etc.



ADC- Data – Register

Register contains AD converter results.

RF - Configuration Register

Register contains transceiver setup information such as frequency and output power ext.

TX – Address

Register contains address of target device. How many bytes used is set in the configuration register.

TX – Payload

Register containing the payload information to be sent in a ShockBurstTM package. How many bytes used is set in the configuration register.

RX – Payload

Register containing the payload information derived from a received valid ShockBurstTM package. How many bytes used is set in the configuration register. Valid data in the RX-Payload register is indicated with a high Data Ready (DR) signal.



11.2 SPI – Instruction Set

The available commands to be used on the SPI-interface are given in Table 21. Whenever CSN is set low the interface would expect an instruction. Every new instruction has to be presided by a high to low transaction on CSN.

Instruction set for the Transceiver and AD converter subsystem		
Instruction Name	Instruction Format	Operation
W_RF_CONFIG (WRC)	0000 AAAA	Write Configuration-register. AAAA indicates which byte the write operation is to be started from. Number of bytes depending on start address AAAA.
R_RF_CONFIG (RRC)	0001 AAAA	Read Configuration-register. AAAA indicates which byte the read operation is to be started from. Number of bytes depending on start address AAAA.
W_TX_PAYLOAD (WTP)	0010 0000	Write TX-payload: 1 – 32 bytes. A write operation will always start at byte 0.
R_TX_PAYLOAD (RTP)	0010 0001	Read TX-payload: 1 – 32 bytes. A read operation will always start at byte 0.
W_TX_ADDRESS (WTA)	0010 0010	Write TX-address: 1 – 4 bytes. A write operation will always start at byte 0.
R_TX_ADDRESS (RTA)	0010 0011	Read TX-address: 1 – 4 bytes. A read operation will always start at byte 0.
R_RX_PAYLOAD (RRP)	0010 0100	Read RX-payload: 1 – 32 bytes. A read operation will always start at byte 0.
R_ADC_DATA (RAD)	0100 000A	Read ADC data. A indicates which byte the read operation is to be started from.
W_ADC_CONFIG (WAC)	0100 0100	Write ADC configuration register: 1 – 3 bytes. A write operation will always start at byte 0.
R_ADC_CONFIG (RAC)	0100 0110	Read ADC configuration register: 1 – 3 bytes. A read operation will always start at byte 0.
CHANNEL_CONFIG (CC)	1000 pphc cccc cccc	Special command for fast setting of CH_NO, HFREQ_PLL and PA_PWR in the CONFIGURATION REGISTER. CH_NO= cccccccc, HFREQ_PLL = h PA_PWR = pp
START_ADC_CONV (SAV)	1100 ssss	Special command for start of an ADC conversion for a given source – ssss = CHSEL.

Table 21 Instruction set for the Transceiver AD converter subsystem.

A read or a write operation may operate on a single byte or on a set of succeeding bytes from a given start address defined by the instruction. When accessing succeeding bytes one will read or write MSB of the byte with the smallest byte number first. The content of the status-register will always be read to MISO after a high to low transition on CSN.



11.3 SPI Timing

Data is clocked into or out of the device on the rising edge of the clock pulse. The clock speed is determined by the MCU and may be from 1Hz to 10MHz depending on the MCU. The device must be in one of the power saving modes for the configuration registers to be read or written to.

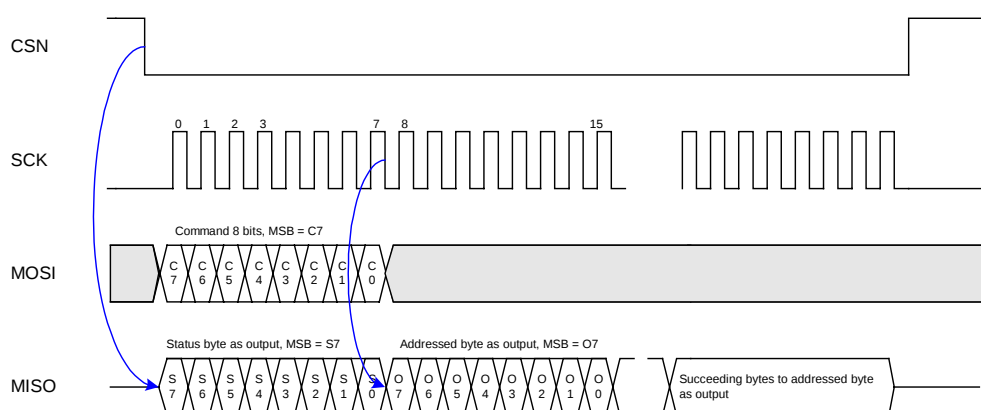


Figure 11 Internal SPI read operation.

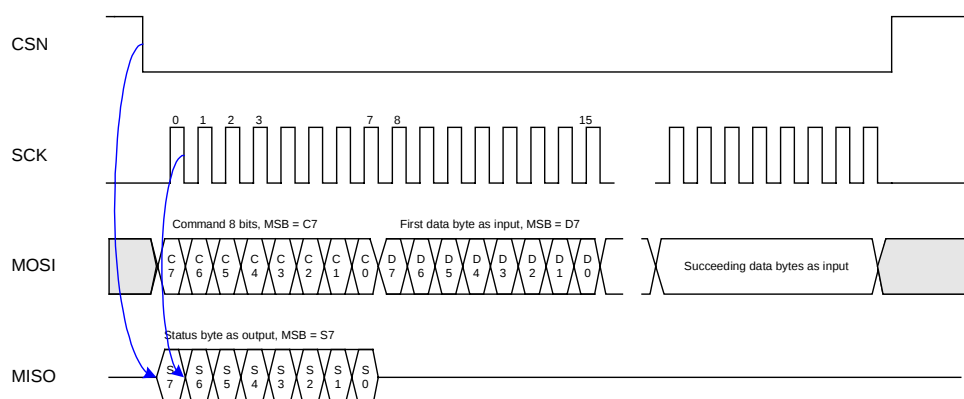


Figure 12 Internal SPI write operation.

The transceiver and AD converter SPI interface is controlled by P2 in the micro controller. That is, SCK, MOSI, MISO and CSN are P2.0, P2.1, P2.2 and P2.3 respectively. Detailed information of mapping is found in chapter 8.



11.4 RF Configuration – Register Description

Parameter	Bitwidth	Description
CH_NO	9	Sets center frequency together with HFREQ_PLL (default value = 001101100 _b = 108 _d). $f_{RF} = (422.4 + CH_NO_d / 10) * (1 + HFREQ_PLL_d)$ MHz
HFREQ_PLL	1	Sets PLL in 433 or 868/915 MHz mode (default value = 0). '0' – Chip operating in 433MHz band '1' – Chip operating in 868 or 915 MHz band
PA_PWR	2	Output power (default value = 00). '00' -10dBm '01' -2dBm '10' +6dBm '11' +10dBm
RX_RED_PWR	1	Reduces current in RX mode by 1.6mA. Sensitivity is reduced (default value = 0). '0' – Normal operation '1' – Reduced power
AUTO_RETRAN	1	Retransmit contents in TX – register as long TRX_CE and TXEN is high (default value = 0). '0' – No retransmission '1' – Retransmission of data package
RX_AFW	3	RX-address width (default value = 100). '001' – 1 byte RX address field width '100' – 4 byte RX address field width
TX_AFW	3	TX-address width (default value = 100). '001' – 1 byte TX address field width '100' – 4 byte TX address field width
RX_PW	6	RX-payload width (default value = 100000). '000001' – 1 byte RX payload field width '000010' – 2 byte RX payload field width '100000' – 32 byte RX payload field width
TX_PW	6	TX-payload width (default value = 100000). '000001' – 1 byte TX payload field width '000010' – 2 byte TX payload field width '100000' – 32 byte TX payload field width
RX_ADDRESS	32	RX address identity. Used bytes depend on RX_AFW (default value = E7E7E7E7 _h).
UP_CLK_FREQ	2	CPU clock frequency (default value = 11). '00' – 4MHz '01' – 2MHz '10' – 1MHz '11' – 500kHz
UP_CLK_EN	1	CPU clock enable (default value = 1). '0' – CPU using UP_CLK_FREQ frequency '1' – CPU using XOF frequency
XOF	3	Crystal oscillator frequency. Must be set according to external crystal resonant-frequency. '000' – 4MHz '001' – 8MHz '010' – 12MHz '011' – 16MHz '100' – 20MHz (default value = 100)
CRC_EN	1	CRC – check enable (default value = 1). '0' – Disable '1' – Enable
CRC_MODE	1	CRC – mode (default value = 1). '0' – 8 CRC check bit '1' – 16 CRC check bit

Table 22 RF configuration-register description.



11.5 ADC - Configuration Register Description

Parameter	Bitwidth	Description
CSTARTN	1	Positive edge of this signal will start one AD conversion when ADCRUN is inactive. This bit is internally synchronized to the ADC clock
ADCRUN	1	ADC running continuously when active. CSTARTN is ignored in this case
ADC_PWR_UP	1	Enable ADC
VFSSEL	1	Select reference for AD converter 0: Use internal band gap reference (nominally 1.22V) 1: Use external pin AREF for reference (ignored if CHSEL=[1xxx]).
CHSEL	4	Channel select input 0000: AIN0 0001: AIN1 0010: AIN2 0011: AIN3 1xxx: internal VDD/3.
RESCTRL	2	Set A/D converter resolution: 00: 6 bit 01: 8 bit 10: 10 bit 11: 12 bit
DIFFMODE,	1	Enable differential measurements, AIN0 must be used as inverting input and one of the other inputs AIN1 to AIN3, as selected by ADCSEL, must be used as noninverting input.
ADC_RL_JUST	1	Select left or right justified data format: 0: Data will be left justified in ADC_DATA_REG 1: Data will be right justified in ADC_DATA_REG

Table 23 ADC Configuration-register description.

11.6 Status-Register Description

Parameter	Bitwidth	Description
AM	1	Address Match, indicate that the receiver has received an address equal to its own identity. Detailed description in chapter 9.8.
CD	1	Carrier Detect, indicates that a carrier is found on the receiving channel. Detailed description in chapter 9.7
DR	1	Data Ready, indicate that the receiver has received a data package with correct address and CRC. Detailed description in chapter 9.9.
EOC	1	End Of Conversion, indicates that an AD conversion is completed and that data is placed in ADC_DATA_REG.
ADC_RFLAG	3	Overflow indication in ADC RFLAG[2]: Underflow (ADCDATA = 0) RFLAG[1]: Overflow (ADCDATA = 2^N-1) RFLAG[0]: Over range = RFLAG[1] or RFLAG[2]

Table 24 Status-register description.



11.7 RF - Register Contents

RF-CONFIG REGISTER (R/W)		
Byte #	Content bit[7:0], MSB = bit[7]	Init value
0	CH_NO[7:0]	0110_1100
1	bit[7:6] not used, AUTO_RETRAN, RX_RED_PWR, PA_PWR[1:0], HFREQ_PLL, CH_NO[8]	0000_0000
2	bit[7] not used, TX_AFW[2:0], bit[3] not used, RX_AFW[2:0]	0100_0100
3	bit[7:6] not used, RX_PW[5:0]	0010_0000
4	bit[7:6] not used, TX_PW[5:0]	0010_0000
5	RX_ADDRESS (device identity) byte 0	E7
6	RX_ADDRESS (device identity) byte 1	E7
7	RX_ADDRESS (device identity) byte 2	E7
8	RX_ADDRESS (device identity) byte 3	E7
9	CRC_MODE, CRC_EN, XOF[2:0], UP_CLK_EN, UP_CLK_FREQ[1:0]	1110_0111

Table 25 RF config register contents.

TX PAYLOAD (R/W)		
Byte #	Content bit[7:0], MSB = bit[7]	Init value
0	TX_PAYLOAD[7:0]	X
1	TX_PAYLOAD[15:8]	X
-	-	X
-	-	X
30	TX_PAYLOAD[247:240]	X
31	TX_PAYLOAD[255:248]	X

Table 26 TX payload register contents.

TX ADDRESS (R/W)		
Byte #	Content bit[7:0], MSB = bit[7]	Init value
0	TX_ADDRESS[7:0]	E7
1	TX_ADDRESS[15:8]	E7
2	TX_ADDRESS[23:16]	E7
3	TX_ADDRESS[31:24]	E7

Table 27 TX address register contents.

RX PAYLOAD (R)		
Byte #	Content bit[7:0], MSB = bit[7]	Init value
0	RX_PAYLOAD[7:0]	X
1	RX_PAYLOAD[15:8]	X
	-	X
	-	X
30	RX_PAYLOAD[247:240]	X
31	RX_PAYLOAD[255:248]	X

Table 28 RX payload register contents.



11.8 ADC Configuration Register Contents

ADC CONFIG REG (R/W)		
Byte #	Content bit[7:0], MSB = bit[7]	Init value
0	Control: CHSEL[7:4], VFSSEL, PWR_UP, ADCRUN, CSTARTN	0000_0001
1	Static: bit[7:4] not used, ADC_RL_JUST, DIFFMODE, RESCTRL[1:0]	0000_0010

Table 29 ADC Configuration Register contents.

11.9 ADC Data Register Contents

ADC DATA REG (R)		
Byte #	Content bit[7:0], MSB = bit[7]	Init value
0	Left or right justified data from ADC	X
1	Left or right justified data from ADC	X

Table 30 ADC DATA Register contents.

11.10 Status Register Contents

STATUS REGISTER (R)		
Byte #	Content bit[7:0], MSB = bit[7]	Init value
0	AM, CD, DR, EOC, ADC_RFLAG[2:0], Even parity	X

Table 31 Status Register contents.

The length of all registers is fixed. However, the bytes in TX_PAYLOAD, RX_PAYLOAD, TX_ADDRESS and RX_ADDRESS used in ShockBurstTM RX/TX are set in the configuration register. Register content is not lost when the device enters one of the power saving modes.



12 TRANCEIVER SUBSYSTEM TIMING

The following timing must be obeyed during nRF905 operation.

12.1 Device Switching Times

nRF905 timing	Max.
STBY → TX Shock Burst™	650 μ s
STBY → RX Shock Burst™	650 μ s
RX Shock Burst™ → TX Shock Burst™	550 μ s
TX Shock Burst™ → RX Shock Burst™	550 μ s

Notes to table:

- 1) RX to TX or TX to RX switching is available without re-programming of the RF configuration register. The same frequency channel is maintained.

Table 32 Switching times for nRF905.

12.2 ShockBurst™ TX Timing

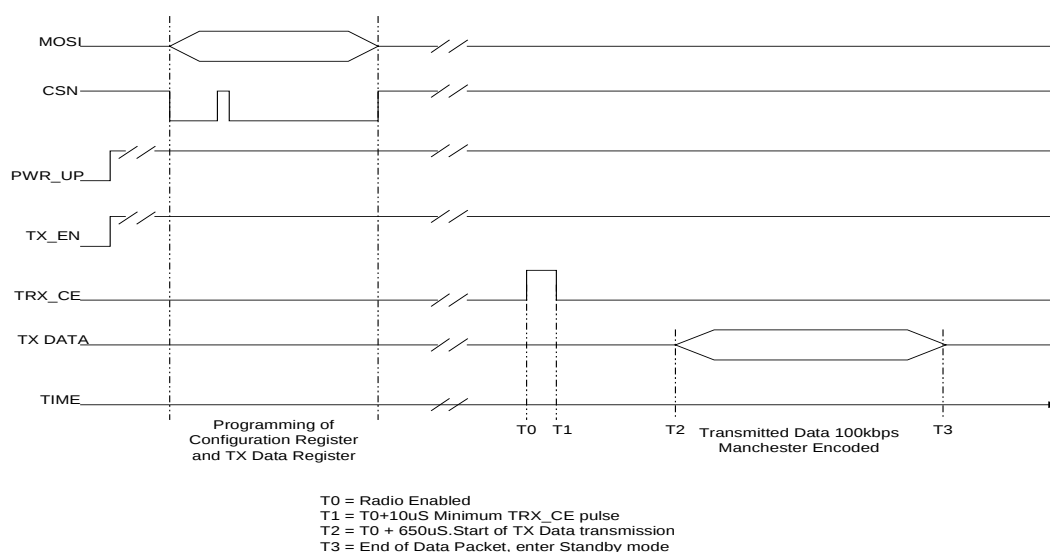


Figure 13 Timing diagram for standby to transmit.

After a data packet has finished transmitting the device will automatically enter Standby mode and wait for the next pulse of TRX_CE. If the Auto Re-Transmit function is enabled the data packet will continue re-sending the same data packet until TRX_CE is set low.



12.3 ShockBurst™ RX Timing

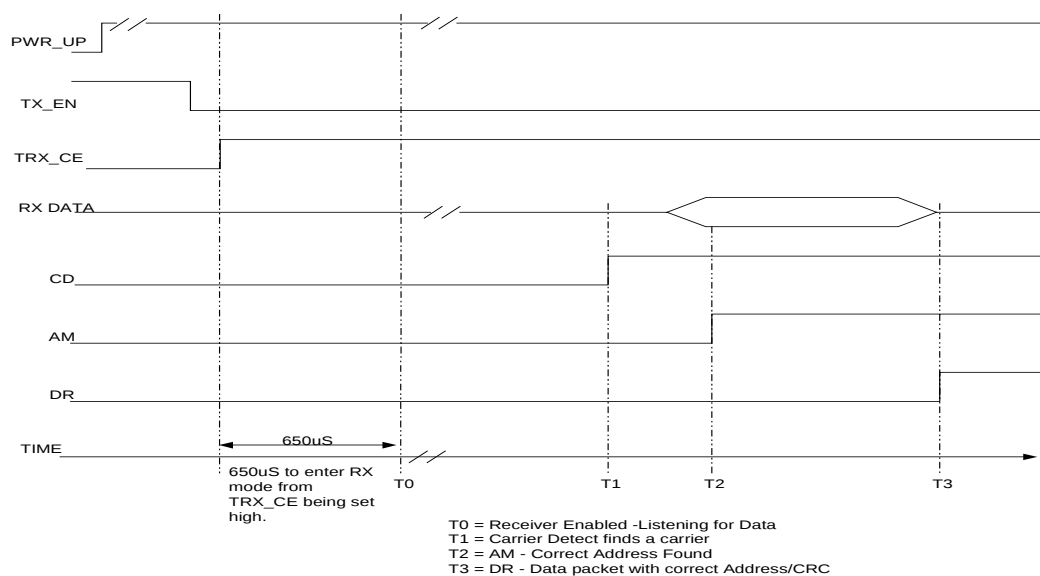


Figure 14 Timing diagram for standby to receiving.

After the Data Ready (DR) has been set high a valid data packet is available in the RX data register. This may be clocked out in Standby mode. After the data has been clocked out via the SPI interface the Data Ready (DR) and Address Match (AM) signals are reset to low.



13 SPI

nRF9E5 SPI is a simple single buffered master. The 3 data lines of the SPI bus (MISO, SCK and MOSI) are multiplexed (by writing to register SPI_CTRL) between the GPIO pins (lower 3 bits of P1) and the RF transceiver and AD converter subsystems. The SPI hardware does not generate any chip select signal. The bootstrap loader uses EECSN (GPIO P0.3) as chip select for the boot EEPROM. On-chip GPIO P2.3 is dedicated as chip select for the RF transceiver and AD converter subsystems. GPIO pins from port 0 may be used as chip selects for other external SPI slaves.

The SPI hardware is controlled by SFR's SPI_DATA (0xb2), SPI_CTRL (0xb3) and SPICLK (0xb4) as explained in Table 33 below.

Addr SFR (hex)	R/W	#bit	Init (hex)	Name	Function
B2	R/W	8	0	SPI_DATA	SPI data input/output
B3	R/W	2	0	SPI_CTRL	00 -> SPI not used no clock generated 01 -> SPI connected to port P1 (as for booting) (see also Table 11 Port 1 (P1) functions) 10 -> SPI connected to the nRF905 transceiver (see Table 15 P2 (RADIO) register)
B4	R/W	4	0	SPICLK	Divider factor from CPU clock to SPI clock 0000: 1/2 of CPU clock frequency 0001: 1/2 of CPU clock frequency 0010: 1/4 of CPU clock frequency 0011: 1/8 of CPU clock frequency 0100: 1/16 of CPU clock frequency 0101: 1/32 of CPU clock frequency 0110: 1/64 of CPU clock frequency other: 1/64 of CPU clock frequency

Table 33 SPI control and data SFR-registers.



14 PWM

The nRF9E5 PWM output is a one-channel PWM with a 2 register interface. The first register, PWMCON, enables PWM function and PWM period length, which is the number of clock cycles for one PWM period, as shown in the table below. The other register, PWMDUTY, controls the duty cycle of the PWM output signal. When this register is written, the PWM signal will change immediately to the new value. This can result in 4 transitions within one PWM period, but the transition period will always have a “DC value” between the “old” sample and the “new” sample.

The table shows how PWM frequency (or period length) and PWM duty cycle are controlled by the settings in the two PWM SFR-registers. For a crystal frequency of 16 MHz, PWM frequency range will be about 1-253 kHz.

PWMCON[7:6] (Number of bits)	PWM frequency	PWMDUTY (duty cycle)
00 (0)	0 (PWM module inactive)	0
01 (6)	$f_{XO} \cdot \frac{1}{63 \cdot (PWMCON[5:0] + 1)}$	$\frac{PWMDUTY[5:0]}{63}$
10 (7)	$f_{XO} \cdot \frac{1}{127 \cdot (PWMCON[5:0] + 1)}$	$\frac{PWMDUTY[6:0]}{127}$
11 (8)	$f_{XO} \cdot \frac{1}{255 \cdot (PWMCON[5:0] + 1)}$	$\frac{PWMDUTY}{255}$

Table 34 PWM frequency and duty-cycle.

PWM is controlled by SFR 0xA9 and 0xAA.

Addr SFR (hex)	R/W	#bit	Init (hex)	Name	Function
A9	R/W	8	0	PWMCON	PWM control register 7-6: Enable / period length select 00: Disable PWM 01: Period length is 6 bit 10: Period length is 7 bit 11: Period length is 8 bit 5-0: PWM frequency prescale factor (see table above)
AA	R/W	8	0	PWMDUTY	PWM duty cycle (6 to 8 bits according to period length)

Table 35 PWM control registers - SFR 0xA9 and 0xAA.



15 INTERRUPTS

nRF9E5 supports the following interrupt sources:

Interrupt signal	Natural Priority	Interrupt Vector	Flag	Enable	Control	Description
INT0_N	1	0x03	TCON.1	IE.0	IP.0	External interrupt, active low, configurable as edge-sensitive or level-sensitive, at Port P0.3
TF0	2	0x0B	TCON.5	IE.1	IP.1	Timer 0 interrupt
INT1_N	3	0x13	TCON.3	IE.2	IP.2	External interrupt, active low, configurable as edge-sensitive or level-sensitive, at Port P0.4
TF1	4	0x1B	TCON.7	IE.3	IP.3	Timer 1 interrupt
TI or RI	5	0x23	SCON.0 (RI), SCON.1 (TI)	IE.4	IP.4	Receive/transmit interrupt from Serial Port
TF2 or EXF2	6	0x2B	T2CON.7 (TF2), T2CON.6 (EXF2)	IE.5	IP.5	Timer 2 interrupt
int2	8	0x43	EXIF.4	EIE.0	EIP.0	Internal ADC EOC (end of AD conversion) interrupt
int3	9	0x4B	EXIF.5	EIE.1	EIP.1	Internal SPI READY interrupt
int4	10	0x53	EXIF.6	EIE.2	EIP.2	Internal Radio Data Ready (DR) interrupt
int5	11	0x5B	EXIF.7	EIE.3	EIP.3	Internal Radio Address Match (AM) interrupt
wdti	12	0x63	EICON.3	EIE.4	EIP.4	Internal Wakeup (GPIO wakeup and RTC timer) interrupt

Table 36 nRF9E5 interrupt sources.

15.1 Interrupt SFRs

The following SFRs are associated with interrupt control:

- IE – SFR 0xA8 (Table 37)
- IP – SFR 0xB8 (Table 38)
- EXIF – SFR 0x91 (Table 39)
- EICON – SFR 0xD8 (Table 40)
- EIE – SFR 0xE8 (Table 41)
- EIP – SFR 0xF8 (Table 42)

The IE and IP SFRs provide interrupt enable and priority control for the standard interrupt unit, as with industry standard 8051. The EXIF, EICON, EIE, and EIP registers provide flags, enable control, and priority control for the extended interrupt unit.



Table 37 explains the bit functions of the IE register.

Bit	Function
IE.7	EA - Global interrupt enable. Controls masking of all interrupts. EA = 0 disables all interrupts (EA overrides individual interrupt enable bits). When EA = 1, each interrupt is enabled or masked by its individual enable bit.
IE.6	Reserved. Read as 0.
IE.5	ET2 - Enable Timer 2 interrupt. ET2 = 0 disables Timer 2 interrupt (TF2). ET2 = 1 enables interrupts generated by the TF2 or EXF2 flag.
IE.4	ES - Enable Serial Port interrupt. ES = 0 disables Serial Port interrupts (TI and RI). ES = 1 enables interrupts generated by the TI or RI flag.
IE.3	ET1 - Enable Timer 1 interrupt. ET1 = 0 disables Timer 1 interrupt (TF1). ET1 = 1 enables interrupts generated by the TF1 flag.
IE.2	EX1 - Enable external interrupt 1. EX1 = 0 disables external interrupt 1 (INT1_N). EX1 = 1 enables interrupts generated by the INT1_N pin.
IE.1	ET0 - Enable Timer 0 interrupt. ET0 = 0 disables Timer 0 interrupt (TF0). ET0 = 1 enables interrupts generated by the TF0 flag.
IE.0	EX0 - Enable external interrupt 0. EX0 = 0 disables external interrupt 0 (INT0_N). EX0 = 1 enables interrupts generated by the INT0_N pin.

Table 37 IE Register – SFR 0xA8.

Table 38 explains the bit functions of the IP register.

Bit	Function
IP.7	Reserved. Read as 1.
IP.6	Reserved. Read as 0.
IP.5	PT2 - Timer 2 interrupt priority control. PT2 = 0 sets Timer 2 interrupt (TF2) to low priority. PT2 = 1 sets Timer 2 interrupt to high priority.
IP.4	PS - Serial Port interrupt priority control. PS = 0 sets Serial Port interrupt (TI or RI) to low priority. PS = 1 sets Serial Port interrupt to high priority.
IP.3	PT1 - Timer 1 interrupt priority control. PT1 = 0 sets Timer 1 interrupt (TF1) to low priority. PT1 = 1 sets Timer 1 interrupt to high priority.
IP.2	PX1 - External interrupt 1 priority control. PX1 = 0 sets external interrupt 1 (INT1_N) to low priority. PT1 = 1 sets external interrupt 1 to high priority.
IP.1	PT0 - Timer 0 interrupt priority control. PT0 = 0 sets Timer 0 interrupt (TF0) to low priority. PT0 = 1 sets Timer 0 interrupt to high priority.
IP.0	PX0 - External interrupt 0 priority control. PX0 = 0 sets external interrupt 0 (INT0_N) to low priority. PT0 = 1 sets external interrupt 0 to high priority.

Table 38 IP Register – SFR 0xB8.



Table 39 explains the bit functions of the EXIF register.

Bit	Function
EXIF.7	IE5 - Interrupt 5 flag. IE5 = 1 indicates that a rising edge was detected on the radio AM signal (see P2). IE5 must be cleared by software. Setting IE5 in software generates an interrupt, if enabled.
EXIF.6	IE4 - Interrupt 4 flag. IE4 = 1 indicates that a rising edge was detected on the radio DR signal (see P2). IE4 must be cleared by software. Setting IE4 in software generates an interrupt, if enabled.
EXIF.5	IE3 - Interrupt 3 flag. IE3 = 1 indicates that the internal SPI module has sent or received 8 bits, and is ready for a new command. IE3 must be cleared by software. Setting IE3 in software generates an interrupt, if enabled.
EXIF.4	IE2 - Interrupt 2 flag. IE2 = 1 indicates that a rising edge was detected on the ADC's EOC signal (see chapter 10). IE2 must be cleared by software. Setting IE2 in software generates an interrupt, if enabled.
EXIF.3	Reserved. Read as 1.
EXIF.2-0	Reserved. Read as 0.

Table 39 EXIF Register – SFR 0x91.

Table 40 explains the bit functions of the EICON register.

Bit	Function
EICON.7	Not used.
EICON.6	Reserved. Read as 1.
EICON.5	Reserved. Read as 0.
EICON.4	Reserved. Read as 0.
EICON.3	WDTI - Wakeup (GPIO wakeup and RTC timer) interrupt flag. WDTI = 1 indicates a wakeup event interrupt was detected. WDTI must be cleared by software before exiting the interrupt service routine. Otherwise, the interrupt occurs again. Setting WDTI in software generates a wakeup event interrupt, if enabled.
EICON.2-0	Reserved. Read as 0.

Table 40 EICON Register – SFR 0xD8.

Table 41 explains the bit functions of the EIE register.

Bit	Function
EIE.7-5	Reserved. Read as 1.
EIE.4	EWDI - Enable RTC wakeup timer interrupt. EWDI = 0 disables wakeup timer interrupt (wdti). EWDI = 1 enables interrupts generated by wakeup.
EIE.3	EX5 - Enable interrupt 5. EX5 = 0 disables interrupt 5 (radio AM (address match)). EX5 = 1 enables interrupts generated by the radio AM signal.
EIE.2	EX4 - Enable interrupt 4. EX4 = 0 disables interrupt 4 (radio DR (data ready)). EX4 = 1 enables interrupts generated by the radio DR signal.
EIE.1	EX3 - Enable interrupt 3. EX3 = 0 disables interrupt 3 (SPI READY). EX3 = 1 enables interrupts generated by the SPI READY signal.
EIE.0	EX2 - Enable interrupt 2. EX2 = 0 disables interrupt 2 (ADC EOC). EX2 = 1 enables interrupts generated by the ADC EOC signal.

Table 41 EIE Register – SFR 0xE8.



Table 42 explains the bit functions of the EIP register.

Bit	Function
EIP.7-5	Reserved. Read as 1.
EIP.4	PWDI - Wakeup interrupt priority control. WDPI = 0 sets the wakeup interrupt (wdti) to low priority. PS = 1 sets wakeup timer interrupt to high priority.
EIP.3	PX5 - interrupt 5 priority control. PX5 = 0 sets interrupt 5 (radio AM) to low priority. PX5 = 1 sets interrupt 5 to high priority.
EIP.2	PX4 - interrupt 4 priority control. PX4 = 0 sets interrupt 4 (radio DR) to low priority. PX4 = 1 sets interrupt 4 to high priority.
EIP.1	PX3 - interrupt 3 priority control. PX3 = 0 sets interrupt 3 (SPI READY) to low priority. PX3 = 1 sets interrupt 3 to high priority.
EIP.0	PX2 - interrupt 2 priority control. PX2 = 0 sets interrupt 2 (ADC EOC) to low priority. PX2 = 1 sets interrupt 2 to high priority.

Table 42 EIP Register – SFR 0xF8.

15.2 Interrupt Processing

When an enabled interrupt occurs, the CPU vectors to the address of the interrupt service routine (ISR) associated with that interrupt, as listed in Table 36. The CPU executes the ISR to completion unless another interrupt of higher priority occurs. Each ISR ends with an RETI (return from interrupt) instruction. After executing the RETI, the CPU returns to the next instruction that would have been executed if the interrupt had not occurred.

An ISR can only be interrupted by a higher priority interrupt. That is, an ISR for a low-level interrupt can be interrupted only by a high-level interrupt. The CPU always completes the instruction in progress before servicing an interrupt. If the instruction in progress is RETI, or a write access to any of the IP, IE, EIP, or EIE SFRs, the CPU completes one additional instruction before servicing the interrupt.

15.3 Interrupt Masking

The EA bit in the IE SFR (IE.7) is a global enable for all interrupts. When EA = 1, each interrupt is enabled/masked by its individual enable bit. When EA = 0, all interrupts are masked. Table 36 provides a summary of interrupt sources, flags, enables, and priorities.

15.4 Interrupt Priorities

There are two stages of interrupt priority assignment: interrupt level and natural priority. The interrupt level (high, or low) takes precedence over natural priority. All interrupts can be assigned either high or low priority. In addition to an assigned priority level (high or low), each interrupt has a natural priority, as listed in Table 36. Simultaneous interrupts with the same priority level (for example, both high) are resolved according to their natural priority. For example, if INT0_N and int2 are both programmed as high priority, INT0_N takes precedence. Once an interrupt is being serviced, only an interrupt of higher priority level can interrupt the service routine of the interrupt currently being serviced.



15.5 Interrupt Sampling

The internal timers and serial port generate interrupts by setting their respective SFR interrupt flag bits. The CPU samples external interrupts once per instruction cycle, at the rising edge of CPU_clk at the end of cycle C4.

The INT0_N and INT1_N signals are both active low and can be programmed through the IT0 and IT1 bits in the TCON SFR to be either edge-sensitive or level-sensitive. For example, when IT0 = 0, INT0_N is level-sensitive and the CPU sets the IE0 flag when the INT0_N pin is sampled low. When IT0 = 1, INT0_N is edge-sensitive and the CPU sets the IE0 flag when the INT0_N pin is sampled high then low on consecutive samples. To ensure that edge-sensitive interrupts are detected, the corresponding ports should be held high for four clock cycles and then low for four clock cycles. Level-sensitive interrupts are not latched and must remain active until serviced.



15.6 Interrupt Latency

Interrupt response time depends on the current state of the CPU. The fastest response time is five instruction cycles: one to detect the interrupt, and four to perform the LCALL to the ISR. The maximum latency (thirteen instruction cycles) occurs when the CPU is currently executing an RETI instruction followed by a MUL or DIV instruction. The thirteen instruction cycles in this case are: one to detect the interrupt, three to complete the RETI, five to execute the DIV or MUL, and four to execute the LCALL to the ISR.

For the maximum latency case, the response time is $13 \times 4 = 52$ clock cycles.

15.7 Interrupt Latency from Power Down State.

The nRF9E5 may be set into Power Down state by writing a non zero value to SFR 0xB6, register CK_CTRL. The CPU will then perform a controlled shutdown of clock and power regulator depending on what mode was selected. The system can only be restarted from an RTC wakeup, a GPIO wakeup or a Watchdog reset. If a wakeup interrupt is enabled, the startup time for regulators and clocks will be added to the interrupt latency. See 17.2.1 Startup Time From Reset

15.8 Single-Step Operation

The nRF9E5 interrupt structure provides a way to perform single-step program execution. When exiting an ISR with an RETI instruction, the CPU will always execute at least one instruction of the task program. Therefore, once an ISR is entered, it cannot be re-entered until at least one program instruction is executed. To perform single-step execution, program one of the external interrupts (for example, INT0_N) to be level sensitive and write an ISR for that interrupt that terminates as follows:

```
JNB TCON.1,$ ;    wait for high on INT0_N
JB TCON.1,$ ;    wait for low on INT0_N
RETI ;           return for ISR
```

The CPU enters the ISR when INT0_N goes low, then waits for a pulse on INT0_N. Each time INT0_N is pulsed, the CPU exits the ISR, executes one program instruction, then re-enters the ISR.



16 LF CLOCK WAKEUP FUNCTIONS AND WATCHDOG

16.1 The LF Clock

The nRF9E5 contains has an internal low frequency clock CKLF that is always active. When the crystal oscillator clocks the circuit, the CKLF is a 4kHz clock derived from the crystal oscillator (provided the CKLFCON register is set according to crystal frequency and prescaler. XOF and UP_CLK_FREQ respectively, see Table 22). When no crystal oscillator clock is available, the CKLF is a low power RC oscillator (LP_OSC) that cannot be disabled, so it will run continuously as long as $VDD \geq 1.8V$.

The microprocessor can determine the phase of the CKLF clock by reading CK_CTRL SFR 0xB6, see Table 50.

16.2 Tick Calibration

The “TICK” is an interval (in CKLF periods) that determines the resolution of the watchdog and the RTC wakeup timer. The tick is nominally 1ms (4 CKLF cycles). When the CPU is active and in power down modes where the chip still has crystal clock, the “TICK” will be as accurate as the crystal oscillator. When the CKLF switches to the RC oscillator (LP_OSC) in deep power down modes, the tick will no longer be accurate. The LP_OSC clock source is very inaccurate, and may vary from 0.5ms to 3ms depending production lot, temperature and supply voltage. That means that Watchdog and RTC wakeup may not be used for any accurate timing functions if these power down modes are used.

The accuracy can be improved by calibrating the TICK value at regular intervals. The register TICK_DV controls how many LP_OSC periods elapse between each TICK. The frequency of the LP_OSC (between 1 kHz and 5 kHz) can be measured by timer2 in capture mode with t2ex enabled (EXEN2=1). The signal connected to t2ex has exactly half the frequency of LP_OSC. The 16-bit difference between two consecutive captures in SFR-registers {RCAP2H, RCAP2L} is proportional to the LP_OSC period. For details about timer2 see ch. 18.8.3 and Figure 21 Timer 2 – Timer/Counter with Capture

TICK is controlled by SFRs 0xB5 and 0xBF

Addr SFR	R/W	#bit	Init Hex	Name	Function
B5	R/W	8	03	TICK_DV	Divider that's used in generating TICK from CKLF frequency. $T_{TICK} = (1 + TICK_DV) / f_{CKLF}$ The default value gives a TICK of 1ms nominal as default (with CKLF derived from crystal oscillator).
BF	R/W	6	27	CKLFCON	Configure CKLF generation with crystal frequency and prescaler value. Note this register only controls the generation of CKLF, not the actual prescaler values. 5-3: Should be set equal to XOF, Table 22 2: Should be set equal to UP_CLK_EN, Table 22 1-0: Should be set equal to UP_CLK_FREQ, Table 22

Table 43 TICK control register - SFR 0xB5.



16.3 RTC Wakeup Timer

The RTC is a simple 24 bit down counter that produces an optional interrupt and reloads automatically when the count reaches zero. This process is initially disabled, and will be enabled with the first write to the lower 16 bit of the timer latch. Writing the lower 16 bits of the timer latch will always be followed by a reload of the counter. Writing the upper 8 bit of the timer latch should only be done when the timer is disabled. The counter may be disabled again by writing a disable opcode to the control register. Both the latch and the counter value may be read by giving the respective codes in the control register, see description in Table 45.

This counter is used for a wakeup sometime in the future (a relative time wakeup call). If 'N' is written to the counter, the first wakeup will happen from somewhere between 'N+1' and 'N+2' "TICK" from the completion of the write, thereafter a new wakeup is issued every "N+1" "TICK" until the unit is disabled or another value is written to the latch.

The wakeup timer is one of the sources that can generate a WDTI interrupt to the CPU. The programmer may poll the EICON.3 flag or enable the interrupt. If the device is in a power down state, the wakeup will force the device to exit power down regardless of the state of EIE.4 interrupt enable.

The nRF9E5 do not provide any "absolute time functions". Absolute time functions in nRF9E5 can well be handled in software since the RAM is continuously powered even when in sleep mode.

16.4 Programmable GPIO Wakeup Function

Any number of the pins in port 0 may be used as wakeup signals for the nRF9E5. The device may be programmed to react on either rising or falling or both edges of each pin individually. Additionally each pin is equipped with a programmable "filter" that can be used for glitch suppression.

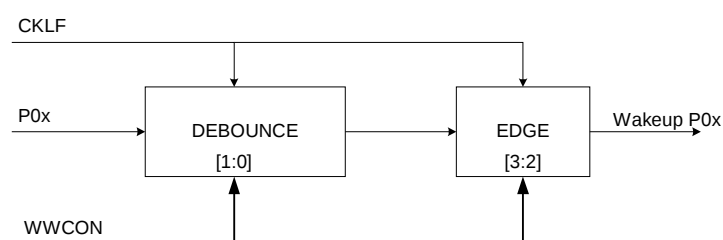


Figure 15 Wakeup filter, each pin for GPIO wakeup function.

The debounce act as a low pass filter. The input has to be stable for a number of clock pulses given for the corresponding change to appear on the output. Edge triggers on either positive, negative or both edges. The edge delay is 2 clock cycles. Please see Table 44 and Table 47 for filter configuration.



Filter selection Debounce		Edge detector selection	
WCON [1:0]	Number of clock pulses	WCON [3:2]	pos / neg trigger
00	0	00	Off
01	2	01	Pos
10	8	10	Neg
11	64	11	Both

Table 44 GPIO wakeup filter configuration.

16.5 Watchdog

The watchdog is activated on the first write to its control register SFR 0xAD. It can not be disabled by any other means than a reset. The watchdog register is loaded by writing a 16-bit value to the two 8-bit data registers (SFR 0xAB and 0xAC) and then the writing the correct opcode to the control register. The watchdog will then count down towards 0 and when 0 is reached the complete microcontroller will be reset. To avoid the reset, the software must load new values into the watchdog register sufficiently often.

16.6 Programming Interface to Watchdog and Wakeup Functions

Figure 16 shows how the blocks that are always active are connected to the CPU. RTC timer GPIO wakeup and Watchdog are controlled via SFRs 0xAB, 0xAC and 0xAD. These 3 registers REGX_MSB, REGX_LSB and REGX_CTRL are used to interface the blocks running on the slow CKLF clock. The 16-bit register {REGX_MSB, REGX_LSB} can be written or read as two bytes from the CPU.



Typical sequences are:

Write: Wait until REGX_CTRL.4 == 0 (i.e. not busy)

Write REGX_MSB, Write REGX_LSB, Write REGX_CTRL

Read: Wait until REGX_CTRL.4 == 0 (i.e. not busy)

Write REGX_CTRL, Wait until REGX_CTRL.4 == 0 (i.e. not busy)

Read REGX_MSB, Read REGX_LSB

Note : Please wait until not busy before accessing SFR 0xB6 CK_CTRL (page 57)

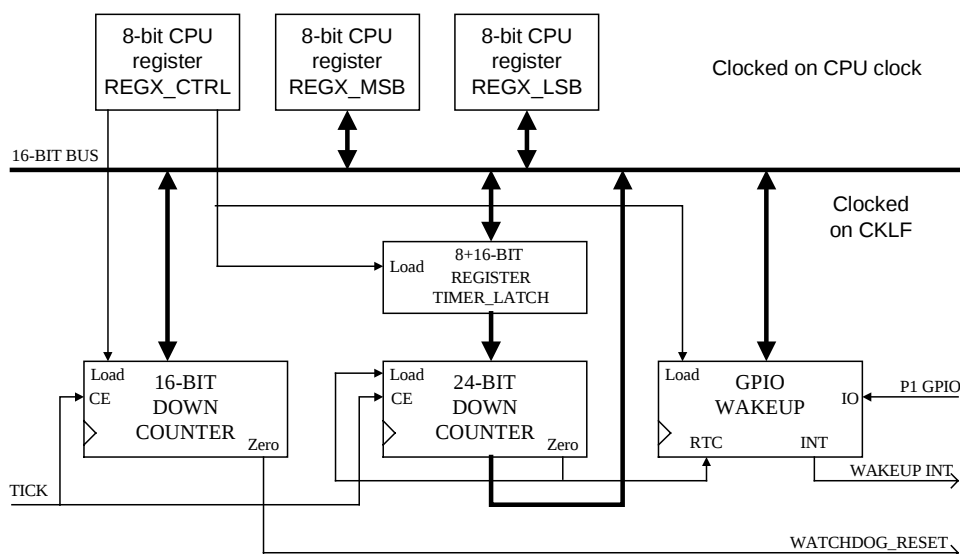


Figure 16 Block diagram of wakeup and watchdog function.

Table 45 below describe the functions of the SFR registers that control these blocks, and Table 46 and Table 47 explains the contents of the individual control registers for watchdog and wakeup functions.

Addr SFR (hex)	R/W	#bit	Init Hex	Name	Function
AB	R/W	8	00	REGX_MSB	Most significant part of 16 bit register for interface to Watchdog, RTC timer and GPIO wakeup
AC	R/W	8	00	REGX_LSB	Least significant part of 16 bit register for interface to Watchdog, RTC timer and GPIO wakeup
AD	R/W	5	00	REGX_CTRL	Control for 16 bit register for transfers to and from Watchdog, RTC timer and GPIO wakeup. 4: REGX interface busy (read only). 3: Read (0) / Write (1) 2-0: Indirect address, see leftmost column in Table 46

Table 45 Wakeup, RTC timer and Watchdog SFR-registers.



Addr Ctrl [2:0]	R/W Ctrl [3]	#bit	Init Hex	Name	Function
0	0	16	0000	RWD	Watchdog register (count)
	1	16	0000	WWD	Watchdog register (count)
1	0	16	0000	RGTIMER	15-8: MSB part of RTC counter 7-0: MSB part of RTC latch
	1	12	000	WGTIMER	11-8: GTIMER latch 7-0: MSB part of RTC latch
2	0	16	0000	RRTCLAT	Least significant part of RTC latch
	1	16	0000	WRTCLAT	Least significant part of RTC latch
3	0	16	0000	RRTC	RTC counter value
	1	0	-	WRTCDIS	Disable RTC (data not used)
4	0	9	000	RWSTA0	Wakeup status Bit 8: RTC timer status 7-0: Wakeup status for pins P07-P00
	1	16	0000	WWCON0	GPIO wakeup configuration for P03-P00. See Table 47.
5	0	9	000	RWSTA1	Wakeup status (Identical to WSTA0)
	1	16	0000	WWCON1	GPIO wakeup configuration for P07-P04. See Table 47.

Table 46 Indirect addresses and functions.

Bits	WWCON1 function	WWCON0 unction
15:14	Edge selection for P07	Edge selection for P03
13:12	Edge filter for P07	Edge filter for P03
11:10	Edge selection for P06	Edge selection for P02
9:8	Edge filter for P06	Edge filter for P02
7:6	Edge selection for P05	Edge selection for P01
5:4	Edge filter for P05	Edge filter for P01
3:2	Edge selection for P04	Edge selection for P00
1:0	Edge filter for P04	Edge filter for P00

Table 47 Bit fields in register WWCON1 and WWCON0.

16.7 Reset

The nRF9E5 can be reset either by the on-chip power-on reset circuitry or by the on-chip watchdog counter.

16.7.1 Power-on Reset

The power-on reset circuitry keeps the chip in power-on-reset state until the supply voltage reaches VDDmin (a voltage, less than 1.9V sufficiently high for digital operation). At this point the internal voltage generators and oscillators start up, the SFRs are initialized to their reset values, as listed in Table 62, and thereafter the CPU begins program execution at the standard reset vector address 0x0000. The startup time from power-on reset is normally determined by both the crystal oscillator startup time and the frequency of the low power oscillator (LP_OSC). This total may vary from 1 to 3 ms depending on processing, temperature and supply voltage.



16.7.2 Watchdog Reset

If the Watchdog reset signal goes active, nRF9E5 enters the same reset sequence as for power-on reset. That is, the internal voltage generators and oscillators start up, the SFRs are initialized to their reset values, as listed in Table 62, and thereafter the CPU begins program execution at the standard reset vector address 0x0000. The startup time from watchdog reset is somewhat shorter; expect a variation from 0.4 to 2ms depending on processing, temperature and supply voltage.

16.7.3 Program Reset Address

The program reset address is controlled by the RSTREAS register, SFR 0xB1, see Table 48. This register shows which reset source that caused the last reset, and provides a choice of two different program start addresses. The default value is power-on reset, which starts the boot loader, while a watchdog reset does not reboot and restarts at address 0 of the already loaded program.

Addr SFR (hex)	R/W	#bit	Init (hex)	Name	Function
B1	R/W	2	02	RSTREAS	bit 0: Reason for last reset 0: POR 1: Any other reset source Clear this bit in software to force a reboot after jump to zero (boot loader will load code RAM if this bit is 0) bit 1: Use IROM for reset vector 0: Reset vectors to 0x0000. 1: Reset vectors to 0x8000.

Table 48 Reset control register - SFR 0xB1.



17 POWER SAVING MODES

nRF9E5 provides the two industry standard 8051 power saving modes: idle mode and stop mode. To Achieve more power saving several additional power-down modes are provided, where both oscillator and internal power regulators may be turned off.

The bits that control entry into idle and stop modes are in the PCON register at SFR address 0x87, listed in Table 49. The bits that control entry into power down mode are in the CK_CTRL register at SFR address 0xB6, listed in Table 51.

Bit	Function
PCON.7	SMOD – Serial Port baud-rate doubler enable. When SMOD = 1, the baud rate for Serial Port is doubled.
PCON.6–4	Reserved.
PCON.3	GF1 – General purpose flag 1. Bit-addressable, general purpose flag for software control.
PCON.2	GF0 – General purpose flag 0. Bit-addressable, general purpose flag for software control.
PCON.1	STOP – Stop mode select. Setting the STOP bit places the nRF9E5 in stop mode.
PCON.0	IDLE – Idle mode select. Setting the IDLE bit places the nRF9E5 in idle mode.

Table 49 PCON Register – SFR 0x87.

17.1 Standard 8051 Power Saving Modes

17.1.1 Idle Mode

An instruction that sets the IDLE bit (PCON.0) causes the nRF9E5 to enter idle mode when that instruction completes. In idle mode, CPU processing is suspended and internal registers and memory maintain their current data. However, unlike the standard 8051, the CPU clock is not disabled internally, thus not much power is saved.

There are two ways to exit idle mode: activate any enabled interrupt or watchdog reset. Activation of any enabled interrupt causes the hardware to clear the IDLE bit and terminate idle mode. The CPU executes the ISR associated with the received interrupt. The RETI instruction at the end of the ISR returns the CPU to the instruction following the one that put the nRF9E5 into idle mode. A watchdog reset causes the nRF9E5 to exit idle mode, reset internal registers, execute its reset sequence and begin program execution at the standard reset vector address 0x0000.

17.1.2 Stop Mode

An instruction that sets the STOP bit (PCON.1) causes the nRF9E5 to enter stop mode when that instruction completes. Stop mode is identical to idle mode, except that the only way to exit stop mode is by watchdog reset. Since there is little power saving, stop mode is not recommended, as it is more efficient to use power down mode.



17.2 Additional Power Down Modes

An instruction that sets the CK_CTRL (SFR 0xB6) to a non zero value causes the nRF9E5 to enter power down mode when that instruction completes. In power down mode, CPU processing is suspended, while internal registers and memories maintain their current data. The CPU will perform a controlled shutdown of clock and power regulators as requested by CK_CTRL.

The device can only be restarted from an event on a P0 GPIO pin, an RTC wakeup or a Watchdog reset. Activation of any enabled wakeup source causes the hardware to clear the CK_CTRL bit and terminate power down mode. If there is an enabled interrupt associated with the wakeup even, the CPU executes the ISR associated with that interrupt immediately after power and clocks are restored. The RETI instruction at the end of the ISR returns the CPU to the instruction following the one that put the nRF9E5 into power down mode. A watchdog reset causes the nRF9E5 to exit power down mode, reset internal registers, execute its reset sequence and begin program execution at the standard reset vector address 0x0000.

Addr SFR	R/W	#bit	Init Hex	Name	Function
B6	W	3	0	CK_CTRL	Set power down according to Table 51.
	R	1	-	CK_CTRL	Read LFCK clock in LSB. Other bits are unpredictable.

Table 50 CK_CTRL register – SFR 0xB6.

Note: Before writing the CK_CTRL register, make sure that the busy bit of RTC/Watchdog SFR 0xAD, bit 4 (page 53) is not set

Note: When using power down modes where the CKLF source is LP_OSC, the startup time may be so long that the CPU may loose the corresponding RTC interrupt.

CK_CTRL (write)	Function	CKLF source	XTAL Osc	Typical Current	Typical Startup
000	Normal operation, active	XTAL	On	1 mA	-
001	Light power down	XTAL	On	0.4 mA	2.5 μ s
010	Moderate power down	XTAL	On	125 μ A	7 μ s
011	Standby mode	LP_OSC	On	25 μ A	150 μ s
1--	Deep power down	LP_OSC	Off	2.5 μ A	1000 μ s

Table 51 Power down modes.

The table above shows typical startup time from RTC interrupt. For GPIO the debounce time must be added, but during debounce the device is still in power down.

17.2.1 Startup Time From Reset

Startup time consists of a number of LP_OSC cycles + a number of XTAL clock cycles. f_{LP_OSC} may vary from 1 to 5.5kHz over voltage and temperature.



Startup times are summarized in the table below:

Reason of startup	Phase I (power and Clock)	Phase II (Initialization and synchronization)
Power on	XO start-up time (3ms max)	The longest of: 2500 f_{XTAL} cycles 0-1 LP_OSC cycles
Watchdog	XO start-up time if not already running	The longest of: 2500 f_{CPU} cycles 0-1 LP_OSC cycles

Table 52 Startup times from Power down mode.



18 MICROCONTROLLER

The embedded microcontroller is the DW8051 MacroCell from Synopsys which is similar to the Dallas DS80C320 in terms of hardware features and instruction-cycle timing.

18.1 Memory Organization

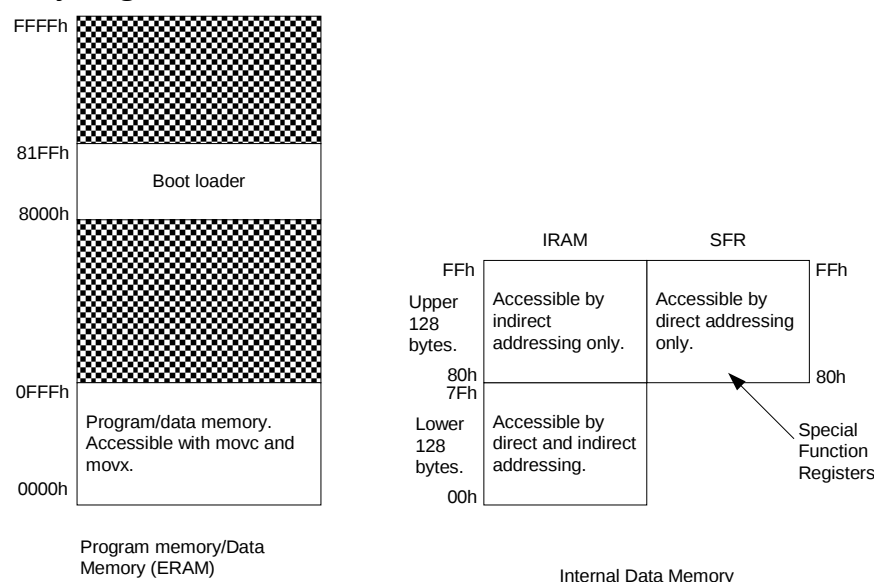


Figure 17 Memory Map and Organization.

18.1.1 Program Memory/Data Memory

The nRF9E5 has 4KB of program memory available for user programs located at the bottom of the address space as shown in Figure 17. This memory also function as a random access memory and can be accessed with the movx and movc instructions.

After power on reset the boot loader loads the user program from the external serial EEPROM and stores it from address 0 in this memory.

18.1.2 Internal Data Memory

The Internal Data Memory, illustrated in Figure 17, consists of:

- 128 bytes of registers and scratchpad memory accessible through direct or indirect addressing (addresses 0x00–0x7F).
- 128 bytes of scratchpad memory accessible through indirect addressing (0x80–0xFF).
- 128 special function registers (SFRs) accessible through direct addressing.

The lower 32 bytes form four banks of eight registers (R0–R7). Two bits on the program status word (PSW) select which bank is in use. The next sixteen bytes form a block of bit-addressable memory space at bit addresses 0x00–0x7F. All of the bytes in the lower 128 bytes are accessible through direct or indirect addressing. The SFRs and the upper 128 bytes of RAM share the same address range (0x80–0xFF). However, the actual address space is separate and is differentiated by the type of addressing. Direct



addressing accesses the SFRs, while indirect addressing accesses the upper 128 bytes of RAM. Most SFRs are reserved for specific functions, as described in 18.6 Special Function Registers on page 68. SFR addresses ending in 0h or 8h are bit-addressable.

18.2 Program Format in External EEPROM

The table below shows the layout of the first few bytes of the EEPROM image.

	7	6	5	4	3	2	1	0
0:	Version (now 00)		Reserved (now 00)		SPEED	XO_FREQ		
1:	Offset to start of user program (N)							
2:	Number of 256 byte blocks in user program (includes block 0 that is not full)							
...	Optional User data, not interpreted by boot loader							
...	...							
N:	First byte of user program, goes into ERAM at 0x0000							
N+1:	Second byte of user program, goes into ERAM at 0x0001							
	...							

Table 53 EEPROM layout.

The contents of the 4 lowest bits in the first byte is used by the boot loader to set the correct SPI frequency. These fields are encoded as shown below:

SPEED (bit 3): EEPROM max speed

0 = 1MHz

1 = 0.5MHz

XO_FREQ (bits 2,1 and 0): Crystal oscillator frequency

000 = 4MHz,

001 = 8MHz,

010 = 12MHz,

011 = 16MHz,

100 = 20MHz

The program `eeprep`¹ can be used to add this header to a program file.

Command format: `eeprep [options] <infile> <outfile>`

<infile> is the output file of an assembler or compiler

<outfile> is a file suitable for programming the EEPROM (above format with no user data).

Both files are "Intelhex" format.

The options available for `eeprep` are:

-c n Set crystal frequency in MHz.

-i Ignore checksums

-p n Set program memory size (default 4096 bytes)

-s Select slow EEPROM clock (500KHz)

¹ Available on www.nvlsi.no



18.3 Instruction Set

All nRF9E5 instructions are binary-code-compatible and perform the same functions that they do in the industry standard 8051. The effects of these instructions on bits, flags, and other status functions is identical to the industry-standard 8051. However, the timing of the instructions is different, both in terms of number of clock cycles per instruction cycle and timing within the instruction cycle.

Table 55 to Table 60 lists the nRF9E5 instruction set and the number of instruction cycles required to complete each instruction.

Symbol	Function
A	Accumulator
Rn	Register R0–R7
direct	Internal register address
@Ri	Internal register pointed to by R0 or R1 (except MOVX)
rel	Two's complement offset byte
bit	Direct bit address
#data	8-bit constant
#data 16	16-bit constant
addr 16	16-bit destination address
addr 11	11-bit destination address

Table 54 Legend for Instruction Set Table.

Table 55 to Table 60 define the symbols and mnemonics used in Table 54.



Arithmetic Instructions				
Mnemonic	Description	Byte	Instr. Cycles	Hex Code
ADD A, Rn	Add register to A	1	1	28–2F
ADD A, direct	Add direct byte to A	2	2	25
ADD A, @Ri	Add data memory to A	1	1	26–27
ADD A, #data	Add immediate to A	2	2	24
ADDC A, Rn	Add register to A with carry	1	1	38–3F
ADDC A, direct	Add direct byte to A with carry	2	2	35
ADDC A, @Ri	Add data memory to A with carry	1	1	36–37
ADDC A, #data	Add immediate to A with carry	2	2	34
SUBB A, Rn	Subtract register from A with borrow	1	1	98–9F
SUBB A, direct	Subtract direct byte from A with borrow	2	2	95
SUBB A, @Ri	Subtract data memory from A with borrow	1	1	96–97
SUBB A, #data	Subtract immediate from A with borrow	2	2	94
INC A	Increment A	1	1	04
INC Rn	Increment register	1	1	08–0F
INC direct	Increment direct byte	2	2	05
INC @Ri	Increment data memory	1	1	06–07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	1	18–1F
DEC direct	Decrement direct byte	2	2	15
DEC @Ri	Decrement data memory	1	1	16–17
INC DPTR	Increment data pointer	1	3	A3
MUL AB	Multiply A by B	1	5	A4
DIV AB	Divide A by B	1	5	84
DA A	Decimal adjust A	1	1	D4
All mnemonics are copyright © Intel Corporation 1980.				

Table 55 nRF9E5 Instruction Set, Arithmetic Instructions.



Logical Instructions				
Mnemonic	Description	Byte	Instr. Cycles	Hex Code
ANL A, Rn	AND register to A	1	1	58–5F
ANL A, direct	AND direct byte to A	2	2	55
ANL A, @Ri	AND data memory to A	1	1	56–57
ANL A, #data	AND immediate to A	2	2	54
ANL direct, A	AND A to direct byte	2	2	52
ANL direct, #data	AND immediate data to direct byte	3	3	53
ORL A, Rn	OR register to A	1	1	48–4F
ORL A, direct	OR direct byte to A	2	2	45
ORL A, @Ri	OR data memory to A	1	1	46–47
ORL A, #data	OR immediate to A	2	2	44
ORL direct, A	OR A to direct byte	2	2	42
ORL direct, #data	OR immediate data to direct byte	3	3	43
XRL A, Rn	Exclusive-OR register to A	1	1	68–6F
XRL A, direct	Exclusive-OR direct byte to A	2	2	65
XRL A, @Ri	Exclusive-OR data memory to A	1	1	66–67
XRL A, #data	Exclusive-OR immediate to A	2	2	64
XRL direct, A	Exclusive-OR A to direct byte	2	2	62
XRL direct, #data	Exclusive-OR immediate to direct byte	3	3	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap nibbles of A	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13
All mnemonics are copyright © Intel Corporation 1980.				

Table 56 nRF9E5 Instruction Set, Logical Instructions.



Boolean Instructions				
Mnemonic	Description	Byte	Instr. Cycles	Hex Code
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	2	C2
SETB C	Set carry	1	1	D3
SETB bit	Set direct bit	2	2	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	2	B2
ANL C, bit	AND direct bit to carry	2	2	82
ANL C, /bit	AND direct bit inverse to carry	2	2	B0
ORL C, bit	OR direct bit to carry	2	2	72
ORL C, /bit	OR direct bit inverse to carry	2	2	A0
MOV C, bit	Move direct bit to carry	2	2	A2
MOV bit, C	Move carry to direct bit	2	2	92
All mnemonics are copyright © Intel Corporation 1980.				

Table 57 nRF9E5 Instruction Set, Boolean Instructions.



Data Transfer Instructions				
Mnemonic	Description	Byte	Instr. Cycles	Hex Code
MOV A, Rn	Move register to A	1	1	E8–EF
MOV A, direct	Move direct byte to A	2	2	E5
MOV A, @Ri	Move data memory to A	1	1	E6–E7
MOV A, #data	Move immediate to A	2	2	74
MOV Rn, A	Move A to register	1	1	F8–FF
MOV Rn, direct	Move direct byte to register	2	2	A8–AF
MOV Rn, #data	Move immediate to register	2	2	78–7F
MOV direct, A	Move A to direct byte	2	2	F5
MOV direct, Rn	Move register to direct byte	2	2	88–8F
MOV direct, direct	Move direct byte to direct byte	3	3	85
MOV direct, @Ri	Move data memory to direct byte	2	2	86–87
MOV direct, #data	Move immediate to direct byte	3	3	75
MOV @Ri, A	Move A to data memory	1	1	F6–F7
MOV @Ri, direct	Move direct byte to data memory	2	2	A6–A7
MOV @Ri, #data	Move immediate to data memory	2	2	76–77
MOV DPTR, #data	Move immediate to data pointer	3	3	90
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	3	93
MOVC A, @A+PC	Move code byte relative PC to A	1	3	83
MOVX A, @Ri	Move external data (A8) to A	1	2–9*	E2–E3
MOVX A, @DPTR	Move external data (A16) to A	1	2–9*	E0
MOVX @Ri, A	Move A to external data (A8)	1	2–9*	F2–F3
MOVX @DPTR, A	Move A to external data (A16)	1	2–9*	F0
PUSH direct	Push direct byte onto stack	2	2	C0
POP direct	Pop direct byte from stack	2	2	D0
XCH A, Rn	Exchange A and register	1	1	C8–CF
XCH A, direct	Exchange A and direct byte	2	2	C5
XCH A, @Ri	Exchange A and data memory	1	1	C6–C7
XCHD A, @Ri	Exchange A and data memory nibble	1	1	D6–D7
All mnemonics are copyright © Intel Corporation 1980.				

Table 58 nRF9E5 Instruction Set, Data Transfer Instructions.

* Number of cycles is 2 + CKCON.2-0. (CKCON.2-0 is the integer value of the 3LSB of SFR 0x8E CKCON). Default is 3 cycles.



Branching Instructions				
Mnemonic	Description	Byte	Instr. Cycles	Hex Code
ACALL addr 11	Absolute call to subroutine	2	3	11–F1
LCALL addr 16	Long call to subroutine	3	4	12
RET	Return from subroutine	1	4	22
RETI	Return from interrupt	1	4	32
AJMP addr 11	Absolute jump unconditional	2	3	01–E1
LJMP addr 16	Long jump unconditional	3	4	02
SJMP rel	Short jump (relative address)	2	3	80
JC rel	Jump on carry = 1	2	3	40
JNC rel	Jump on carry = 0	2	3	50
JB bit, rel	Jump on direct bit = 1	3	4	20
JNB bit, rel	Jump on direct bit = 0	3	4	30
JBC bit, rel	Jump on direct bit = 1 and clear	3	4	10
JMP @A+DPTR	Jump indirect relative DPTR	1	3	73
JZ rel	Jump on accumulator = 0	2	3	60
JNZ rel	Jump on accumulator != 0	2	3	70
CJNE A, direct, rel	Compare A, direct JNE relative	3	4	B5
CJNE A, #d, rel	Compare A, immediate JNE relative	3	4	B4
CJNE Rn, #d, rel	Compare reg, immediate JNE relative	3	4	B8–BF
CJNE @Ri, #d, rel	Compare ind, immediate JNE relative	3	4	B6–B7
DJNZ Rn, rel	Decrement register, JNZ relative	2	3	D8–DF
DJNZ direct, rel	Decrement direct byte, JNZ relative	3	4	D5
All mnemonics are copyright © Intel Corporation 1980.				

Table 59 nRF9E5 Instruction Set, Branching Instructions.

Miscellaneous Instructions				
Mnemonic	Description	Byte	Instr. Cycles	Hex Code
NOP	No operation	1	1	00
There is an additional reserved opcode (A5) that will also act as a NOP. All mnemonics are copyright © Intel Corporation 1980.				

Table 60 nRF9E5 Instruction Set, Miscellaneous Instructions.



18.4 Instruction Timing

Instruction cycles in the nRF9E5 are four clock cycles in length, as opposed to twelve clock cycles per instruction cycle in the standard 8051. This translates to a 3X improvement in execution time for most instructions. However, some instructions require a different number of instruction cycles on the nRF9E5 than they do on the standard 8051. In the standard 8051, all instructions except for MUL and DIV take one or two instruction cycles to complete. In the nRF9E5 architecture, instructions can take between one and five instruction cycles to complete. For example, in the standard 8051, the instructions MOVX A, @DPTR and MOV direct, direct each take two instruction cycles (twenty-four clock cycles) to execute. In the nRF9E5 architecture, MOVX A, @DPTR takes two instruction cycles (eight clock cycles) and MOV direct, direct takes three instruction cycles (twelve clock cycles). Both instructions execute faster on the nRF9E5 than they do on the standard 8051, but require different numbers of clock cycles.

For timing of real-time events, use the numbers of instruction cycles from Table 55 to Table 60 to calculate the timing of software loops. The bytes column of these table indicates the number of memory accesses (bytes) needed to execute the instruction. In most cases, the number of bytes is equal to the number of instruction cycles required to complete the instruction. However, as indicated in Table 55, there are some instructions (for example, DIV and MUL) that require a greater number of instruction cycles than memory accesses. By default, the nRF9E5 timer/counters run at twelve clock cycles per increment so that timer-based events have the same timing as with the standard 8051. The timers can be configured to run at four clock cycles per increment to take advantage of the higher speed of the nRF9E5.

18.5 Dual Data Pointers

The nRF9E5 employs dual data pointers to accelerate data memory block moves. The standard 8051 data pointer (DPTR) is a 16-bit value used to address external data RAM or peripherals. The nRF9E5 maintains the standard data pointer as DPTR0 at SFR locations 0x82 and 0x83. It is not necessary to modify code to use DPTR0. The nRF9E5 adds a second data pointer (DPTR1) at SFR locations 0x84 and 0x85. The SEL bit in the DPTR Select register, DPS (SFR 0x86), selects the active pointer. When SEL = 0, instructions that use the DPTR will use DPL0 and DPH0. When SEL = 1, instructions that use the DPTR will use DPL1 and DPH1. SEL is the bit 0 of SFR location 0x86. No other bits of SFR location 0x86 are used. All DPTR-related instructions use the currently selected data pointer. To switch the active pointer, toggle the SEL bit. The fastest way to do so is to use the increment instruction (INC DPS). This requires only one instruction to switch from a source address to a destination address, saving application code from having to save source and destination addresses when doing a block move. Using dual data pointers provides significantly increased efficiency when moving large blocks of data.

The SFR locations related to the dual data pointers are:

- 0x82 DPL0 DPTR0 low byte
- 0x83 DPH0 DPTR0 high byte
- 0x84 DPL1 DPTR1 low byte
- 0x85 DPH1 DPTR1 high byte
- 0x86 DPS DPTR Select (LSB)



18.6 Special Function Registers

The Special Function Registers (SFRs) control several of the features of the nRF9E5. Most of the nRF9E5 SFRs are identical to the standard 8051 SFRs. However, there are additional SFRs that control features that are not available in the standard 8051. Table 61 lists the nRF9E5 SFRs and indicates which SFRs are not included in the standard 8051 SFR space. When writing software for the nRF9E5, use equate statements to define the SFRs that are specific to the nRF9E5 and custom peripherals. In Table 61, SFR bit positions that contain a 0 or a 1 cannot be written to and, when read, always return the value shown (0 or 1). SFR bit positions that contain “–” are available but not used. Table 62 shows the value of each SFR, after power-on reset or a watchdog reset, together with a pointer to a detailed description of each register. Please note that any unused address in the SFR address space is reserved and should not be written to.

Notes to Table 61 on next page :

- (1) Not part of standard 8051 architecture.
- (2) Registers unique to nRF9E5
- (3) P0, P1 and P3 differ from standard 8051



Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x80	P0(3)	Port 0							
0x81	SP	Stack pointer							
0x82	DPL0	Data pointer 0, low byte							
0x83	DPH0	Data pointer 0, high byte							
0x84	DPL1(1)	Data pointer 1, low byte							
0x85	DPH1(1)	Data pointer 1, high byte							
0x86	DPS(1)	0	0	0	0	0	0	0	SEL
0x87	PCON	SMOD	-	1	1	GF1	GF0	STOP	IDLE
0x88	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
0x89	TMOD	GATE	C/T	M1	M0	GATE	C/T	M1	M0
0x8A	TL0	Timer/counter 0 value, low byte							
0x8B	TL1	Timer/counter 1 value, low byte							
0x8C	TH0	Timer/counter 0 value, high byte							
0x8D	TH1	Timer/counter 1 value, high byte							
0x8E	CKCON(1)	-	-	T2M	T1M	T0M	MD2	MD1	MD0
0x8F	SPC_FNC(1)	0	0	0	0	0	0	0	WRS
0x90	P1(3)	-	-	-	-	Port 1 bit 3:0			
0x91	EXIF(1)	IE5	IE4	IE3	IE2	1	0	0	0
0x92	MPAGE(1)	-	-	-	-	-	-	-	-
0x93	P0_DRV(2)	Drive Strength of port 0							
0x94	P0_DIR(2)	Direction of Port 0							
0x95	P0_ALT(2)	Alternate functions of Port 0							
0x96	P1_DIR(2)	-	-	-	-	Direction of Port 1			
0x97	P1_ALT(2)	-	-	-	-	Alt.funct.of Port 1			
0x98	SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
0x99	SBUF	Serial port data buffer							
0xA0	P2(3)	AM	CD	DR/ TRX_CE	EOC/ TX_EN	SBCSN	SBMISO	SBMOSI	SBCK
0xA8	IE	EA	0	ET2	ES	ET1	EX1	ET0	EX0
0xA9	PWMCON(2)	PWM_LENGTH		PWM_PRESCALE					
0xAA	PWMDUTY(2)	PWM_DUTY_CYCLE							
0xAB	REGX_MSB(2)	High byte of Watchdog/RTC register							
0xAC	REGX_LSB(2)	Low byte of Watchdog/RTC register							
0xAD	REGX_CTRL(2)	-	-	-	Control of REGX_MSB and REGX_LSB				
0xB1	RSTREAS(2)	-	-	-	-	-	-	RFLR	
0xB2	SPI_DATA(2)	SPI_DATA input/output bits							
0xB3	SPI_CTRL(2)	-	-	-	-	-	SPI_CTRL		
0xB4	SPICLK(2)	-	-	-	-	SPICLK			
0xB5	TICK_DV(2)	TICK_DV							
0xB6	CK_CTRL(2)	-	-	-	-	-	CK_CTRL		
0xB8	IP	1	0	PT2	PS	PT1	PX1	PT0	PX0
0xBF	CKLFCON (2)	-	-	XOF			UP_CLK_EN	UP_CLK_FREQ	
0xC8	T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
0xCA	RCAP2L	Timer/counter 2 capture or reload, low byte							
0xCB	RCAP2H	Timer/counter 2 capture or reload, high byte							
0xCC	TL2	Timer/counter 2 value, low byte							
0xCD	TH2	Timer/counter 2 value, high byte							
0xD0	PSW	CY	AC	F0	RS1	RS0	OV	F1	P
0xD8	EICON(1)	-	1	0	0	WDTI	0	0	0
0xE0	ACC	Accumulator register							
0xE8	EIE(1)	1	1	1	EWDI	EX5	EX4	EX3	EX2
0xF0	B	B-register							
0xF8	EIP(1)	1	1	1	PWDI	PX5	PX4	PX3	PX2
0xFE	HWREV (2)	Device hardware revision number							
0xFF	-----	Reserved, do not use							

Table 61 Special Function Registers summary.



Register	Addr	Reset value	Description
ACC	0xE0	0x00	Accumulator register
B	0xF0	0x00	B-register
CK_CTRL	0xB6	0x00	Table 51, page 57
CKCON	0x8E	0x01	Table 67, page 77
CKLFCON	0xBF	0x27	Table 43 on page 50
DPH0	0x83	0x00	ch.18.5, page 67
DPH1	0x85	0x00	ch.18.5, page 67
DPL0	0x82	0x00	ch.18.5, page 67
DPL1	0x84	0x00	ch.18.5, page 67
DPS	0x86	0x00	ch.18.5, page 67
EICON	0xD8	0x40	Table 40, page 46
EIE	0xE8	0xE0	Table 41, page 46
EIP	0xF8	0xE0	Table 42, page 47
EXIF	0x91	0x08	Table 39, page 46
HWREV	0xFE	0x00, read only	hardware revision no
IE	0xA8	0x00	Table 37, page 45
IP	0xB8	0x80	Table 38, page 45
MPAGE	0x92	0x00	do not use
P0	0x80	0xFF	Table 10, page 15
P0_ALT	0x95	0x00	Table 10, page 15
P0_DIR	0x94	0xFF	Table 10, page 15
P0_DRV	0x93	0x00	Table 10, page 15
P1	0x90	0xFF	Table 12, page 16
P1_ALT	0x97	0x00	Table 12, page 16
P1_DIR	0x96	0xF4	Table 12, page 16
P2	0xA0	0x08	Table 15, page 18
PCON	0x87	0x30	Table 49, page 56
PSW	0xD0	0x00	Table 63, page 71
PWMCON	0xA9	0x00	Table 35, page 43
PWMDUTY	0xAA	0x00	Table 35, page 43
RCAP2H	0xCB	0x00	ch.18.8.3.3, page 79
RCAP2L	0xCA	0x00	ch.18.8.3.3, page 79
REGX_CTRL	0xAD	0x00	Table 45, page 53
REGX_LSB	0xAC	0x00	Table 45, page 53
REGX_MSB	0xAB	0x00	Table 45, page 53
RSTREAS	0xB1	0x02	Table 48, page 55
SBUF	0x99	0x00	ch.18.9, page 80
SCON	0x98	0x00	Table 71, page 81
SP	0x81	0x07	Stack pointer
SPC_FNC	0x8F	0x00	do not use
SPI_CTRL	0xB3	0x00	Table 33, page 42
SPI_DATA	0xB2	0x00	Table 33, page 42
SPICLK	0xB4	0x00	Table 33, page 42
T2CON	0xC8	0x00	Table 68, page 78
TCON	0x88	0x00	Table 66, page 74
TH0	0x8C	0x00	ch.18.8, page 73
TH1	0x8D	0x00	ch.18.8, page 73
TH2	0xCD	0x00	ch.18.8, page 73
TICK_DV	0xB5	0x1D	Table 43, page 50
TL0	0x8A	0x00	ch.18.8, page 73
TL1	0x8B	0x00	ch.18.8, page 73
TL2	0xCC	0x00	ch.18.8, page 73
TMOD	0x89	0x00	Table 65, page 73

Table 62 Special Function Register reset values and description, alphabetically.



Table 63 lists the functions of the bits in the PSW register.

Bit	Function
PSW.7	CY - Carry flag. Set to 1 when last arithmetic operation resulted in a carry (during addition) or borrow (during subtraction); otherwise cleared to 0 by all arithmetic operations.
PSW.6	AC - Auxiliary carry flag. Set to 1 when last arithmetic operation resulted in a carry into (during addition) or borrow from (during subtraction) the high-order nibble; otherwise cleared to 0 by all arithmetic operations.
PSW.5	F0 - User flag 0. Bit-addressable, general purpose flag for software control.
PSW.4	RS1 - Register bank select bit 1. Used with RS0 to select a register bank in internal RAM.
PSW.3	RS0 - Register bank select bit 0, decoded as: RS1 RS0 Bank selected 0 0 Register bank 0, addresses 0x00-0x07 0 1 Register bank 1, addresses 0x08-0x0F 1 0 Register bank 2, addresses 0x10-0x17 1 1 Register bank 3, addresses 0x18-0x1F
PSW.2	OV - Overflow flag. Set to 1 when last arithmetic operation resulted in a carry (addition), borrow (subtraction), or overflow (multiply or divide); otherwise cleared to 0 by all arithmetic operations.
PSW.1	F1 - User flag 1. Bit-addressable, general purpose flag for software control.
PSW.0	P - Parity flag. Set to 1 when modulo-2 sum of 8 bits in accumulator is 1 (odd parity); cleared to 0 on even parity.

Table 63 PSW Register – SFR 0xD0.



18.7 SFR Registers Unique to nRF9E5

The table below lists the SFR registers that are unique to nRF9E5 (not part of standard 8051 register map) The registers P0, P1 and P2 (radio) use the addresses for the ports P0, P1 and P2 in a standard 8051. Whereas the functionality of these ports is similar to that of the corresponding ports in standard 8051, it is not identical.

Addr SFR	R/W	#bit	Init hex	Name	Function
80*	R/W	8	FF	P0	Port 0, pins P07 to P00
90*	R/W	8(4)	FF	P1**	Port 1, pins SPI_CSN, SPI_MISO, SPI_MOSI and SPI_SCK
94	R/W	8	FF	P0_DIR	Direction of each GPIO bit of port 0
95	R/W	8	00	P0_ALT	Select alternate functions for each pin of port 0
96	R/W	8(4)	F4	P1_DIR	Direction for each GPIO bit of port 1
97	R/W	8(4)	00	P1_ALT	Select alternate functions for each pin of port 1
A0*	R/W	8	08	P2	General purpose IO for interface to nRF905 radio, for details see chapter 8.1
A9	R/W	8	0	PWMCON	PWM control register
AA	R/W	8	0	PWMDUTY	PWM duty cycle
AB	R/W	8	0	REGX_MSB	High part of 16 bit register for interface to Watchdog and RTC
AC	R/W	8	0	REGX_LSB	Low part of 16 bit register for interface to Watchdog and RTC
AD	R/W	5	0	REGX_CTRL	Control of interface to Watchdog and RTC.
B1	R/W	2	02	RSTREAS	Reset status and control
B2	R/W	8	0	SPI_DATA	SPI data input/output
B3	R/W	2	0	SPI_CTRL	00 -> SPI not used 01 -> connect to P1 10 or 11 -> connect to RADIO
B4	R/W	2	0	SPICLK	Divider from CPU clock to SPI clock
B5	R/W	8	1D	TICK_DV	TICK Divider.
B6	W	3	0	CK_CTRL	Clock control
B7	R	4	0	TEST_MODE	Test mode register. This register must always be 0 in normal mode.
BF	R/W	6	27	CKLFCON	Control generation of 4 kHz CKLF
FE	R	8	00	HWREV	Silicon stepping

Table 64 SFR registers unique to nRF9E5.

* This bit addressable register differs in usage from “standard 8051

** Only 4 lower bits are meaningful in P1 and corresponding P1_DIR and P1_ALT



18.8 Timers/Counters

The nRF9E5 includes three timer/counters (Timer 0, Timer 1 and Timer 2). Each timer/counter can operate as either a timer with a clock rate based on the CPU clock, or as an event counter clocked by the t0 pin (Timer 0), t1 pin (Timer 1), or the t2 pin (Timer 2). These pins are alternate function bits of Port 0 and 1 as this : t0 is P0.5, t1 is P0.6 and t2 is P1.0, for details please see ch. 6.3 on page 15.

Each timer/counter consists of a 16-bit register that is accessible to software as three SFRs: (Table 61)

Timer 0 - TL0 and TH0

Timer 1 - TL1 and TH1

Timer 2 - TL2 and TH2

18.8.1 Timers 0 and 1

Timers 0 and 1 each operate in four modes, as controlled through the TMOD SFR (Table 65) and the TCON SFR (Table 66). The four modes are:

- 13-bit timer/counter (mode 0)
- 16-bit timer/counter (mode 1)
- 8-bit counter with auto-reload (mode 2)
- Two 8-bit counters (mode 3, Timer 0 only)

Bit	Function
TMOD.7	GATE - Timer 1 gate control. When GATE = 1, Timer 1 will clock only when external interrupt INT1_N = 1 and TR1 (TCON.6) = 1. When GATE = 0, Timer 1 will clock only when TR1 = 1, regardless of the state of INT1_N.
TMOD.6	C/T - Counter/Timer select. When C/T = 0, Timer 1 is clocked by CPU_clk/4 or CPU_clk/12, depending on the state of T1M (CKCON.4). When C/T = 1, Timer 1 is clocked by the t1 pin.
TMOD.5	M1 - Timer 1 mode select bit 1.
TMOD.4	M0 - Timer 1 mode select bit 0, decoded as: M1 M0 Mode 00 Mode 0 : 13-bit counter 01 Mode 1 : 16-bit counter 10 Mode 2 : 8-bit counter with auto-reload 11 Mode 3 : Two 8-bit counters
TMOD.3	GATE - Timer 0 gate control. When GATE = 1, Timer 0 will clock only when external interrupt INT0_N = 1 and TR0 (TCON.4) = 1. When GATE = 0, Timer 0 will clock only when TR0 = 1, regardless of the state of INT0_N.
TMOD.2	C/T - Counter/Timer select. When C/T = 0, Timer 0 is clocked by CPU_clk/4 or CPU_clk/12, depending on the state of T0M (CKCON.3). When C/T = 1, Timer 0 is clocked by the t0 pin.
TMOD.1	M1 - Timer 0 mode select bit 1.
TMOD.0	M0 - Timer 0 mode select bit 0, decoded as: M1 M0 Mode 00 Mode 0 : 13-bit counter 01 Mode 1 : 16-bit counter 10 Mode 2 : 8-bit counter with auto-reload 11 Mode 3 : Two 8-bit counters

Table 65 TMOD Register – SFR 0x89.



Bit	Function
TCON.7	TF1 - Timer 1 overflow flag. Set to 1 when the Timer 1 count overflows and cleared when the CPU vectors to the interrupt service routine.
TCON.6	TR1 - Timer 1 run control. Set to 1 to enable counting on Timer 1.
TCON.5	TF0 - Timer 0 overflow flag. Set to 1 when the Timer 0 count overflows and cleared when the CPU vectors to the interrupt service routine.
TCON.4	TR0 - Timer 0 run control. Set to 1 to enable counting on Timer 0.
TCON.3	IE1 - Interrupt 1 edge detect. If external interrupt 1 is configured to be edge-sensitive (IT1 = 1), IE1 is set by hardware when a negative edge is detected on the INT1_N external interrupt pin and is automatically cleared when the CPU vectors to the corresponding interrupt service routine. In edge-sensitive mode, IE1 can also be cleared by software. If external interrupt 1 is configured to be level-sensitive (IT1 = 0), IE1 is set when the INT1_N pin is low and cleared when the INT1_N pin is high. In level-sensitive mode, software cannot write to IE1.
TCON.2	IT1 - Interrupt 1 type select. When IT1 = 1, the nRF9E5 detects external interrupt pin INT1_N on the falling edge (edge-sensitive). When IT1 = 0, the nRF9E5 detects INT1_N as a low level (level-sensitive).
TCON.1	IE0 - Interrupt 0 edge detect. If external interrupt 0 is configured to be edge-sensitive (IT0 = 1), IE0 is set by hardware when a negative edge is detected on the INT0_N external interrupt pin and is automatically cleared when the CPU vectors to the corresponding interrupt service routine. In edge-sensitive mode, IE0 can also be cleared by software. If external interrupt 0 is configured to be level-sensitive (IT0 = 0), IE0 is set when the INT0_N pin is low and cleared when the INT0_N pin is high. In level-sensitive mode, software cannot write to IE0.
TCON.0	IT0 - Interrupt 0 type select. When IT1 = 1, the nRF9E5 detects external interrupt INT0_N on the falling edge (edge-sensitive). When IT1 = 0, the nRF9E5 detects INT0_N as a low level (level-sensitive).

Table 66 TCON Register – SFR 0x88.

18.8.1.1 Mode 0

Mode 0 operation, illustrated in Figure 18, is the same for Timer 0 and Timer 1. In mode 0, the timer is configured as a 13-bit counter that uses bits 0–4 of TL0 (or TL1) and all eight bits of TH0 (or TH1). The timer enable bit (TR0/TR1) in the TCON SFR starts the timer. The C/T bit selects the timer/counter clock source, CPU_clk or T0/T1. The timer counts transitions from the selected source as long as the GATE bit is 0, or the GATE bit is 1 and the corresponding interrupt pin (INT0_N or INT1_N) is deasserted. INT0_N and INT1_N are alternate function bits of Port0, please see Table 8 Port functions. When the 13-bit count increments from 0x1FFF (all ones), the counter rolls over to all zeros, the TF0 (or TF1) bit is set in the TCON SFR, and the t0_out (or t1_out) pin goes high for one clock cycle. The upper three bits of TL0 (or TL1) are indeterminate in mode 0 and must be masked when the software evaluates the register.

18.8.1.2 Mode 1

Mode 1 operation is the same for Timer 0 and Timer 1. In mode 1, the timer is configured as a 16-bit counter. As illustrated in, all eight bits of the LSB register (TL0 or TL1) are used. The counter rolls over to all zeros when the count increments from 0xFFFF. Otherwise, mode 1 operation is the same as mode 0.

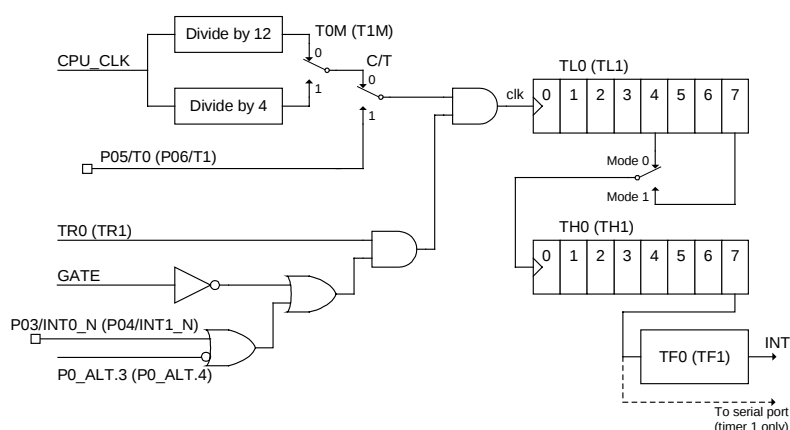


Figure 18 Timer 0/1 – Modes 0 and 1.

18.8.1.3 Mode 2

Mode 2 operation is the same for Timer 0 and Timer 1. In mode 2, the timer is configured as an 8-bit counter, with automatic reload of the start value. The LSB register (TL0 or TL1) is the counter, and the MSB register (TH0 or TH1) stores the reload value. As illustrated in Figure 19 Timer 0/1 – Mode 2, mode 2 counter control is the same as for mode 0 and mode 1. However, in mode 2, when TLn increments from 0xFF, the value stored in THn is reloaded into TLn .

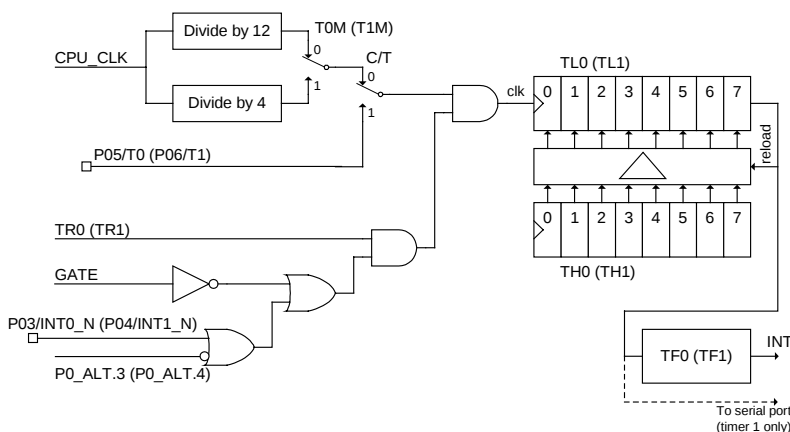


Figure 19 Timer 0/1 – Mode 2.



18.8.1.4 Mode 3

In mode 3, Timer 0 operates as two 8-bit counters, and Timer 1 stops counting and holds its value. As shown in Figure 20 Timer 0 – Mode 3, TL0 is configured as an 8-bit counter controlled by the normal Timer 0 control bits. TL0 can count either CPU clock cycles (divided by 4 or by 12) or high-to-low transitions on t0, as determined by the C/T bit. The GATE function can be used to give counter enable control to the INT0_N signal.

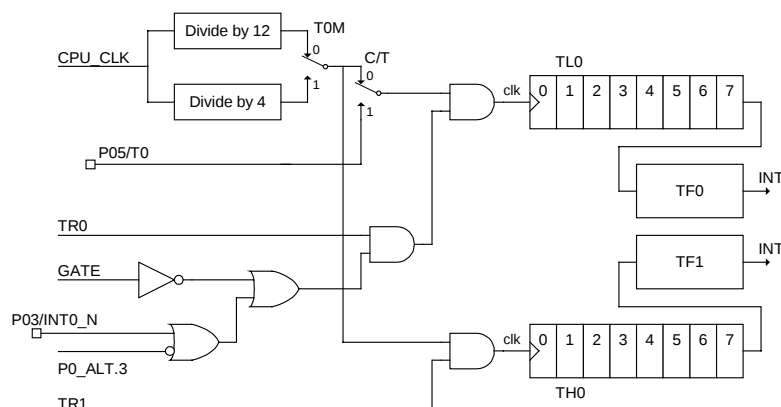


Figure 20 Timer 0 – Mode 3.

TH0 functions as an independent 8-bit counter. However, TH0 can count only CPU clock cycles (divided by 4 or by 12). The Timer 1 control and flag bits (TR1 and TF1) are used as the control and flag bits for TH0.

When Timer 0 is in mode 3, Timer 1 has limited usage because Timer 0 uses the Timer 1 control bit (TR1) and interrupt flag (TF1). Timer 1 can still be used for baud rate generation and the Timer 1 count values are still available in the TL1 and TH1 registers. Control of Timer 1 when Timer 0 is in mode 3 is through the Timer 1 mode bits. To turn Timer 1 on, set Timer 1 to mode 0, 1, or 2. To turn Timer 1 off, set it to mode 3. The Timer 1 C/T bit and T1M bit are still available to Timer 1. Therefore, Timer 1 can count CPU_clk/4, CPU_clk/12, or high-to-low transitions on the t1 pin. The Timer 1 GATE function is also available when Timer 0 is in mode 3.

18.8.2 Timer Rate Control

The default timer clock scheme for the nRF9E5 timers is twelve CPU clock cycles per increment, the same as in the standard 8051. However, in the nRF9E5, the instruction cycle is four clock cycles.

Using the default rate (twelve clocks per timer increment) allows existing application code with real-time dependencies, such as baud rate, to operate properly. However, applications that require fast timing can set the timers to increment every four clock cycles by setting bits in the Clock Control register (CKCON) at SFR location 0x8E, described in Table 67 CKCON Register – SFR 0x.

The CKCON bits that control the timer clock rates are:

CKCON bit Counter/Timer

5	Timer 2
4	Timer 1
3	Timer 0

When a CKCON register bit is set to 1, the associated counter increments at four-clock intervals. When a CKCON bit is cleared, the associated counter increments at twelve-clock intervals. The timer controls are independent of each other. The default setting for



all three timers is 0; that is, twelve-clock intervals. These bits have no effect in counter mode.

Bit	Function
CKCON.7,6	Reserved
CKCON.5	T2M – Timer 2 clock select. When T2M = 0, Timer 2 uses CPU_clk/12 (for compatibility with 80C32); when T2M = 1, Timer 2 uses CPU_clk/4. This bit has no effect when Timer 2 is configured for baud rate generation.
CKCON.4	T1M – Timer 1 clock select. When T1M = 0, Timer 1 uses CPU_clk/12 (for compatibility with 80C32); when T1M = 1, Timer 1 uses CPU_clk/4.
CKCON.3	T0M – Timer 0 clock select. When T0M = 0, Timer 0 uses CPU_clk/12 (for compatibility with 80C32); when T0M = 1, Timer 0 uses CPU_clk/4.
CKCON.2–0	MD2, MD1, MD0 – Control the number of cycles to be used for external MOVX instructions; number of cycles is $2 + \{MD2, MD1, MD0\}$

Table 67 CKCON Register – SFR 0x8E.

default initial data value is 0x01, i.e. MOVX takes 3 cycles.

18.8.3 Timer 2

Timer 2 runs only in 16-bit mode and offers several capabilities not available with Timers 0 and 1. The modes available with Timer 2 are:

- 16-bit timer/counter
- 16-bit timer with capture
- 16-bit auto-reload timer/counter
- Baud-rate generator

The SFRs associated with Timer 2 are:

- T2CON – SFR 0xC8; refer to Table 68 T2CON Register – SFR 0x
- RCAP2L – SFR 0xCA – Used to capture the TL2 value when Timer 2 is configured for capture mode, or as the LSB of the 16-bit reload value when Timer 2 is configured for auto-reload mode.
- RCAP2H – SFR 0xCB – Used to capture the TH2 value when Timer 2 is configured for capture mode, or as the MSB of the 16-bit reload value when Timer 2 is configured for auto-reload mode.

TL2 – SFR 0xCC – Lower eight bits of the 16-bit count.

TH2 – SFR 0xCD – Upper eight bits of the 16-bit count.



Bit	Function
T2CON.7	TF2 - Timer 2 overflow flag. Hardware will set TF2 when Timer 2 overflows from 0xFFFF. TF2 must be cleared to 0 by the software. TF2 will only be set to a 1 if RCLK and TCLK are both cleared to 0. Writing a 1 to TF2 forces a Timer 2 interrupt if enabled.
T2CON.6	EXF2 - Timer 2 external flag. Hardware will set EXF2 when a reload or capture is caused by a high-to-low transition on the t2ex pin, and EXEN2 is set. EXF2 must be cleared to 0 by the software. Writing a 1 to EXF2 forces a Timer 2 interrupt if enabled.
T2CON.5	RCLK - Receive clock flag. Determines whether Timer 1 or Timer 2 is used for Serial port timing of received data in serial mode 1 or 3. RCLK = 1 selects Timer 2 overflow as the receive clock. RCLK = 0 selects Timer 1 overflow as the receive clock.
T2CON.4	TCLK - Transmit clock flag. Determines whether Timer 1 or Timer 2 is used for Serial port timing of transmit data in serial mode 1 or 3. TCLK = 1 selects Timer 2 overflow as the transmit clock. TCLK = 0 selects Timer 1 overflow as the transmit clock.
T2CON.3	EXEN2 - Timer 2 external enable. EXEN2 = 1 enables capture or reload to occur as a result of a high-to-low transition on t2ex, if Timer 2 is not generating baud rates for the serial port. EXEN2 = 0 causes Timer 2 to ignore all external events at t2ex.
T2CON.2	TR2 - Timer 2 run control flag. TR2 = 1 starts Timer 2. TR2 = 0 stops Timer 2.
T2CON.1	C/T2 - Counter/timer select. C/T2 = 0 selects a timer function for Timer 2. C/T2 = 1 selects a counter of falling transitions on the t2 pin. When used as a timer, Timer 2 runs at four clocks per increment or twelve clocks per increment as programmed by CKCON.5, in all modes except baud-rate generator mode. When used in baud-rate generator mode, Timer 2 runs at two clocks per increment, independent of the state of CKCON.5.
T2CON.0	CP/RL2 - Capture/reload flag. When CP/RL2 = 1, Timer 2 captures occur on high-to-low transitions of t2ex, if EXEN2 = 1. When CP/RL2 = 0, auto-reloads occur when Timer 2 overflows or when high-to-low transitions occur on t2ex, if EXEN2 = 1. If either RCLK or TCLK is set to 1, CP/RL2 will not function, and Timer 2 will operate in auto-reload mode following each overflow.

Table 68 T2CON Register – SFR 0xC8.

18.8.3.1 Timer 2 Mode Control

Table 69 summarizes how the SFR bits determine the Timer 2 mode.

RCLK	TCLK	CP/RL2	TR2	Mode
0	0	1	1	16-bit timer/counter with capture
0	0	0	1	16-bit timer/counter with auto-reload
1	X	X	1	Baud-rate generator
X	1	X	1	Baud-rate generator
X	X	X	0	Off

Table 69 Timer 2 Mode Control Summary.

18.8.3.2 16-Bit Timer/Counter Mode

Figure 21 Timer 2 – Timer/Counter with Capture illustrates how Timer 2 operates in timer/counter mode with the optional capture feature. The C/T2 bit determines whether the 16-bit counter counts clock cycles (divided by 4 or 12), or high-to-low transitions on the t2 pin. The TR2 bit enables the counter. When the count increments from 0xFFFF, the TF2 flag is set, and t2_out goes high for one clock cycle.

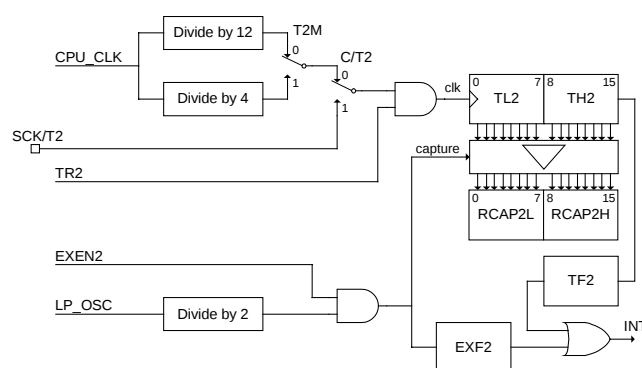


Figure 21 Timer 2 – Timer/Counter with Capture.

18.8.3.3 16-Bit Timer/Counter Mode with Capture

The Timer 2 capture mode, illustrated in Figure 21 Timer 2 – Timer/Counter with Capture, is the same as the 16-bit timer/counter mode, with the addition of the capture registers and control signals. The CP/RL2 bit in the T2CON SFR enables the capture feature. When CP/RL2 = 1, a high-to-low transition on t2ex when EXEN2 = 1 causes the Timer 2 value to be loaded into the capture registers (RCAP2L and RCAP2H).

18.8.3.4 16-Bit Timer/Counter Mode with Auto-Reload

When CP/RL2 = 0, Timer 2 is configured for the auto-reload mode illustrated in Figure 22 Timer 2 – Timer/Counter with Auto-Reload. Control of counter input is the same as for the other 16-bit counter modes. When the count increments from 0xFFFF, Timer 2 sets the TF2 flag and the starting value is reloaded into TL2 and TH2. The software must preload the starting value into the RCAP2L and RCAP2H registers.

When Timer 2 is in auto-reload mode, a reload can be forced by a high-to-low transition on the t2ex pin, if enabled by EXEN2 = 1.

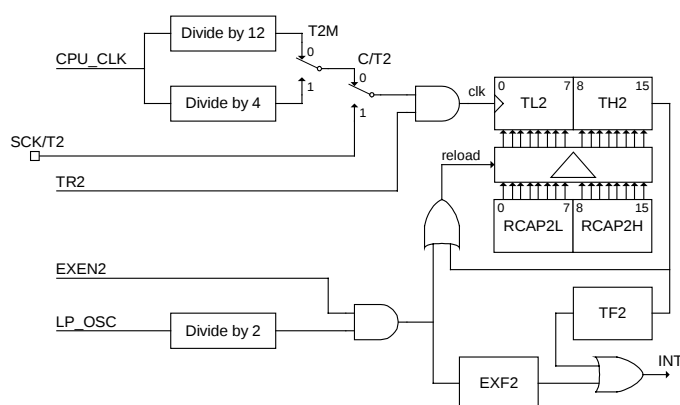


Figure 22 Timer 2 – Timer/Counter with Auto-Reload.



18.8.3.5 Baud Rate Generator Mode

Setting either RCLK or TCLK to 1 configures Timer 2 to generate baud rates for Serial port in serial mode 1 or 3. In baud-rate generator mode, Timer 2 functions in auto-reload mode. However, instead of setting the TF2 flag, the counter overflow generates a shift clock for the serial port function. As in normal auto-reload mode, the overflow also causes the preloaded start value in the RCAP2L and RCAP2H registers to be reloaded into the TL2 and TH2 registers.

When either TCLK = 1 or RCLK = 1, Timer 2 is forced into auto-reload operation, regardless of the state of the CP/RL2 bit.

When operating as a baud rate generator, Timer 2 does not set the TF2 bit. In this mode, a Timer 2 interrupt can be generated only by a high-to-low transition on the t2ex pin setting the EXF2 bit, and only if enabled by EXEN2 = 1. The counter time base in baud-rate generator mode is CPU_clk/2. To use an external clock source, set C/T2 to 1 and apply the desired clock source to the t2 pin.

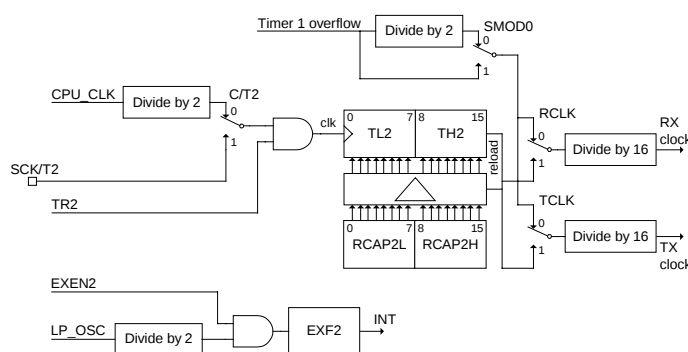


Figure 23 Timer 2 – Baud Rate Generator Mode.

18.9 Serial Interface

The nRF9E5 is configured with one serial port, which is identical in operation to the standard 8051 serial port. The two serial port pins rxd and txd are available as alternate functions of P0.1 and P0.2, for details please see ch. 6.3 on page 15.

The serial port can operate in synchronous or asynchronous mode. In synchronous mode, the nRF9E5 generates the serial clock and the serial port operates in half-duplex mode. In asynchronous mode, the serial port operates in full-duplex mode. In all modes, the nRF9E5 buffers receive data in a holding register, enabling the UART to receive an incoming word before the software has read the previous value.

The serial port can operate in one of four modes, as outlined in Table 70.



Mode	Sync/Async	Baud Clock	Data Bits	Start/ Stop	9th Bit Function
0	Sync	CPU_clk/4 or CPU_clk/12	8	None	None
1	Async	Timer 1 or Timer 2	8	1 start, 1 stop	None
2	Async	CPU_clk/32 or CPU_clk/64	9	1 start, 1 stop	0, 1, parity
3	Async	Timer 1 or Timer 2	9	1 start, 1 stop	0, 1, parity

Table 70 Serial Port Modes.

The SFRs associated with the serial port are:

- SCON – SFR 0x98 – Serial port control (Table 71)
- SBUF – SFR 0x99 – Serial port buffer

Bit	Function															
SCON.7	SM0 - Serial port mode bit 0.															
SCON.6	SM1 - Serial port mode bit 1, decoded as: <table><tr><td>SM0</td><td>SM1</td><td>Mode</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>2</td></tr><tr><td>1</td><td>1</td><td>3</td></tr></table>	SM0	SM1	Mode	0	0	0	0	1	1	1	0	2	1	1	3
SM0	SM1	Mode														
0	0	0														
0	1	1														
1	0	2														
1	1	3														
SCON.5	SM2 - Multiprocessor communication enable. In modes 2 and 3, SM2 enables the multiprocessor communication feature. If SM2 = 1 in mode 2 or 3, RI will not be activated if the received 9 th bit is 0. If SM2 = 1 in mode 1, RI will be activated only if a valid stop is received. In mode 0, SM2 establishes the baud rate: when SM2 = 0, the baud rate is CPU_clk/12; when SM2 = 1, the baud rate is CPU_clk/4.															
SCON.4	REN - Receive enable. When REN = 1, reception is enabled.															
SCON.3	TB8 - Defines the state of the 9 th data bit transmitted in modes 2 and 3.															
SCON.2	RB8 - In modes 2 and 3, RB8 indicates the state of the 9 th bit received. In mode 1, RB8 indicates the state of the received stop bit. In mode 0, RB8 is not used.															
SCON.1	TI - Transmit interrupt flag. Indicates that the transmit data word has been shifted out. In mode 0, TI is set at the end of the 8 th data bit. In all other modes, TI is set when the stop bit is placed on the txd pin. TI must be cleared by the software.															

Table 71 SCON Register – SFR 0x98.

18.9.1 Mode 0

Serial mode 0 provides synchronous, half-duplex serial communication. For Serial Port 0, both serial data input and output occur on rxd pin, and txd provides the shift clock for both transmit and receive. The rxd and txd pins are alternate function bits of Port 0, please also see Table 9 Port 0 (P0) functions for port and pin configuration. The lack of open drain ports on nRF9E5 makes it a programmer responsibility to control the direction of the rxd pin.



The serial mode 0 baud rate is either CPU_clk/12 or CPU_clk/4, depending on the state of the SM2. When SM2 = 0, the baud rate is CPU_clk/12; when SM2 = 1, the baud rate is CPU_clk/4.

Mode 0 operation is identical to the standard 8051. Data transmission begins when an instruction writes to the SBUF SFR. The UART shifts the data out, LSB first, at the selected baud rate, until the 8-bit value has been shifted out.

Mode 0 data reception begins when the REN bit is set and the RI bit is cleared in the corresponding SCON SFR. The shift clock is activated and the UART shifts data in on each rising edge of the shift clock until eight bits have been received. One machine cycle after the 8th bit is shifted in, the RI bit is set and reception stops until the software clears the RI bit.

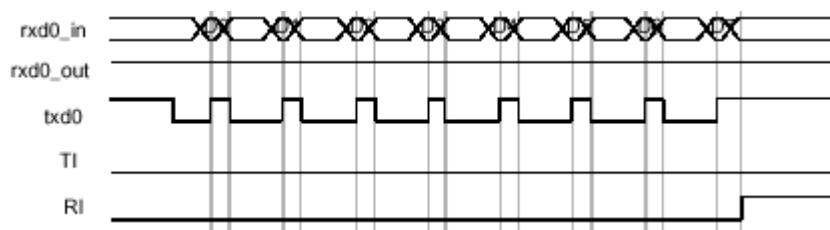


Figure 24 Serial Port Mode 0 receive timing for low-speed (CPU_clk/12) operation.

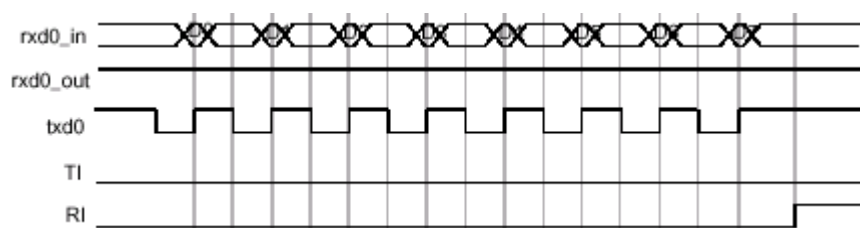


Figure 25 Serial Port Mode 0 receive timing for high-speed (CPU_clk/4) operation.

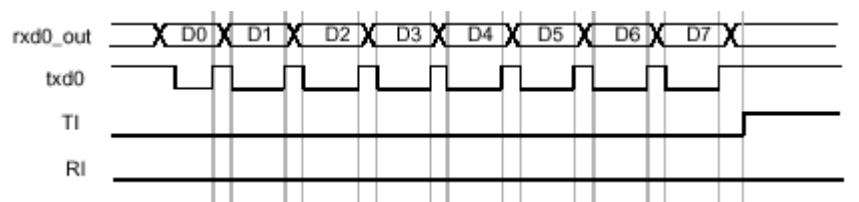


Figure 26 Serial Port Mode 0 transmit timing for high-speed (CPU_clk/4) operation.

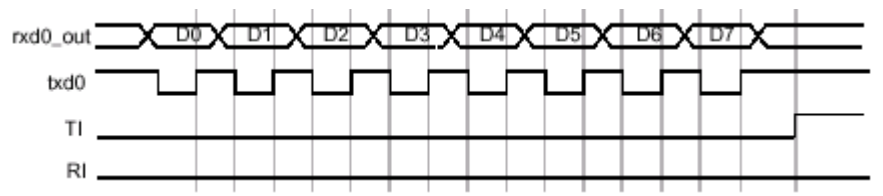


Figure 27 Serial Port Mode 0 transmit timing for high-speed (CPU_clk/4) operation.

**18.9.2 Mode 1**

Mode 1 provides standard asynchronous, full-duplex communication, using a total of ten bits: one start bit, eight data bits, and one stop bit. For receive operations, the stop bit is stored in RB8. Data bits are received and transmitted LSB first.

18.9.2.1 Mode 1 Baud Rate

The mode 1 baud rate is a function of timer overflow. Serial port can use either Timer 1 or Timer 2 to generate baud rates. Each time the timer increments from its maximum count (0xFF for Timer 1 or 0xFFFF for Timer 2), a clock is sent to the baud-rate circuit. The clock is then divided by 16 to generate the baud rate. When using Timer 1, the SMOD bit selects whether or not to divide the Timer 1 rollover rate by 2. Therefore, when using Timer 1, the baud rate is determined by the equation:

$$\text{Baud Rate} = \frac{2^{SMOD}}{32} \times \text{Timer 1 Overflow}$$

SMOD is SFR bit PCON.7

When using Timer 2, the baud rate is determined by the equation:

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow}}{16}$$

To use Timer 1 as the baud-rate generator, it is best to use Timer 1 mode 2 (8-bit counter with auto-reload), although any counter mode can be used. The Timer 1 reload value is stored in the TH1 register, which makes the complete formula for Timer 1:

$$\text{Baud Rate} = \frac{2^{SMOD}}{32} \times \frac{\text{clk}}{4 \times (256 - \text{TH1})}$$

The 4 in the denominator in the above equation can be obtained by setting the T1M bit in the CKCON SFR. To derive the required TH1 value from a known baud rate (when TM1 = 0), use the equation:

$$\text{TH1} = 256 - \frac{2^{SMOD} * \text{clk}}{128 * \text{Baud Rate}}$$

You can also achieve very low serial port baud rates from Timer 1 by enabling the Timer 1 interrupt, configuring Timer 1 to mode 1, and using the Timer 1 interrupt to initiate a 16-bit software reload. Table 72 lists sample reload values for a variety of common serial port baud rates.



Desired Baud Rate	SMOD	C/T	Timer 1 Mode	TH1 Value for 16 MHz CPU clk	TH1 Value for 8 MHz CPU clk
19.2 Kb/s	1	0	2	0xF3	-
9.6 Kb/s	1	0	2	0xE6	0xF3
4.8 Kb/s	1	0	2	0XcC	0xE6
0.4 Kb/s	1	0	2	0x98	0xCC
1.2 Kb/s	1	0	2	0x30	0x98

Table 72 Timer 1 Reload Values for Serial Port Mode 1 Baud Rates.

To use Timer 2 as the baud-rate generator, configure Timer 2 in auto-reload mode and set the TCLK and/or RCLK bits in the T2CON SFR. TCLK selects Timer 2 as the baud-rate generator for the transmitter; RCLK selects Timer 2 as the baud-rate generator for the receiver. The 16-bit reload value for Timer 2 is stored in the RCAP2L and RCA2H SFRs, which makes the equation for the Timer 2 baud rate:

$$\text{Baud Rate} = \frac{clk}{32 \times (65536 - \{RCAP2H, RCAP2L\})}$$

where RCAP2H,RCAP2L is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned number. The 32 in the denominator is the result of the CPU_clk signal being divided by 2 and the Timer 2 overflow being divided by 16. Setting TCLK or RCLK to 1 automatically causes the CPU_clk signal to be divided by 2, as shown in Figure 23 Timer 2 – Baud Rate Generator Mode, instead of the 4 or 12 determined by the T2M bit in the CKCON SFR.

To derive the required RCAP2H and RCAP2L values from a known baud rate, use the equation:

$$RCAP2H, RCAP2L = 65536 - \frac{clk}{32 \times \text{Baud Rate}}$$

Table Table 73 lists sample values of RCAP2L and RCAP2H for a variety of desired baud rates.

Baud Rate	C/T 2	16 MHz CPU clk	
		RCAP2H	RCAP2L
57.6 Kb/s	0	0xFF	0xF7
19.2 Kb/s	0	0xFF	0xE6
9.6 Kb/s	0	0xFF	0xCC
4.8 Kb/s	0	0xFF	0x98
0.4 Kb/s	0	0xFF	0x30
1.2 Kb/s	0	0xFE	0x5F

Table 73 Timer 2 Reload Values for Serial Port Mode 1 Baud Rates.

When either RCLK or TCLK is set, the TF2 flag will not be set on a Timer 2 rollover, and the t2ex reload trigger is disabled.



18.9.2.2 Mode 1 Transmit

Figure 28 illustrates the mode 1 transmit timing. In mode 1, the UART begins transmitting after the first rollover of the divide-by-16 counter after the software writes to the SBUF register. The UART transmits data on the txd pin in the following order: start bit, eight data bits (LSB first), stop bit. The TI bit is set two clock cycles after the stop bit is transmitted.

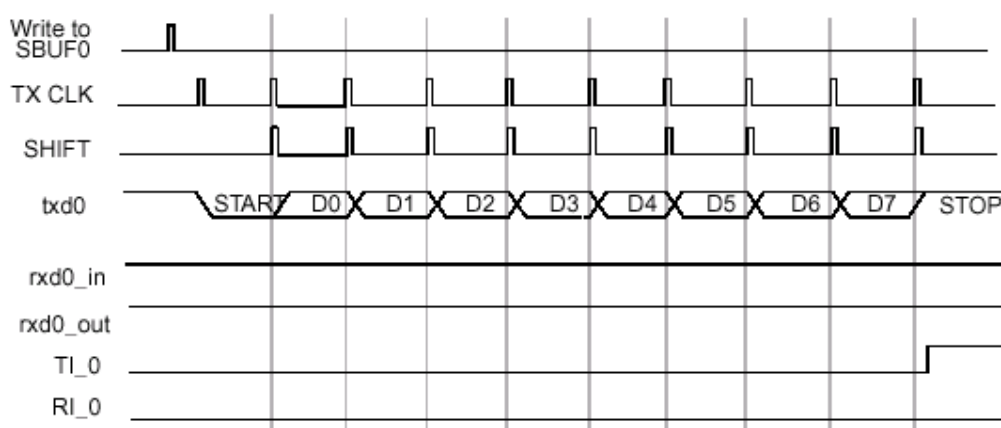


Figure 28 Serial port Mode 1 Transmit Timing.

18.9.2.3 Mode 1 Receive

Figure 29 illustrates the mode 1 receive timing. Reception begins at the falling edge of a start bit received on rxd_in, when enabled by the REN bit. For this purpose, rxd_in is sampled sixteen times per bit for any baud rate. When a falling edge of a start bit is detected, the divide-by-16 counter used to generate the receive clock is reset to align the counter rollover to the bit boundaries.

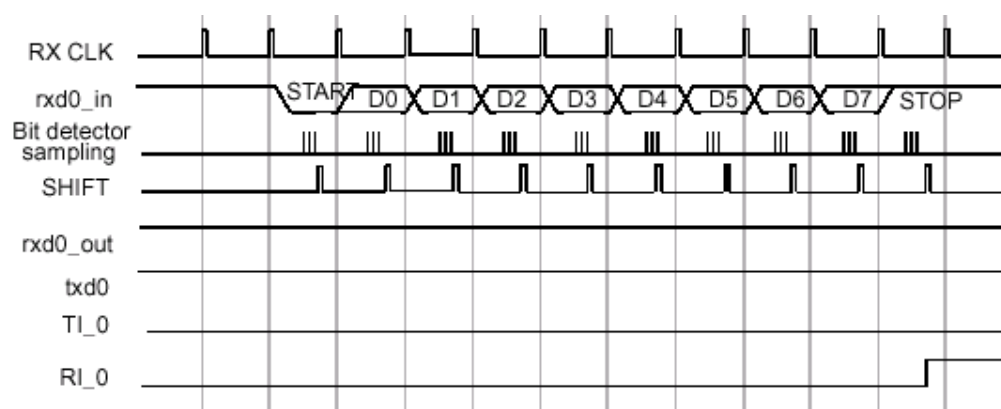


Figure 29 Serial port Mode 1 Receive Timing.



For noise rejection, the serial port establishes the content of each received bit by a majority decision of three consecutive samples in the middle of each bit time. This is especially true for the start bit. If the falling edge on rxd_in is not verified by a majority decision of three consecutive samples (low), then the serial port stops reception and waits for another falling edge on rxd_in.

At the middle of the stop bit time, the serial port checks for the following conditions:

- RI = 0
- If SM2 = 1, the state of the stop bit is 1
(if SM2 = 0, the state of the stop bit does not matter)

If the above conditions are met, the serial port then writes the received byte to the SBUF register, loads the stop bit into RB8, and sets the RI bit. If the above conditions are not met, the received data is lost, the SBUF register and RB8 bit are not loaded, and the RI bit is not set. After the middle of the stop bit time, the serial port waits for another high-to-low transition on the rxd_in pin.

Mode 1 operation is identical to that of the standard 8051 when Timers 1 and 2 use CPU_clk/12 (the default).

18.9.3 Mode 2

Mode 2 provides asynchronous, full-duplex communication, using a total of eleven bits:

- One start bit
- Eight data bits
- One programmable 9th bit
- One stop bit

The data bits are transmitted and received LSB first. For transmission, the 9th bit is determined by the value in TB8. To use the 9th bit as a parity bit, move the value of the P bit (SFR PSW.0) to TB8.

The mode 2 baud rate is either CPU_clk/32 or CPU_clk/64, as determined by the SMOD bit. The formula for the mode 2 baud rate is:

$$\text{Baud Rate} = \frac{2^{\text{SMOD}} * \text{clk}}{64}$$

Mode 2 operation is identical to the standard 8051.

18.9.3.1 Mode 2 Transmit

Figure 30 illustrates the mode 2 transmit timing. Transmission begins after the first rollover of the divide-by-16 counter following a software write to SBUF. The UART shifts data out on the txd pin in the following order: start bit, data bits (LSB first), 9th bit, stop bit. The TI bit is set when the stop bit is placed on the txd pin.

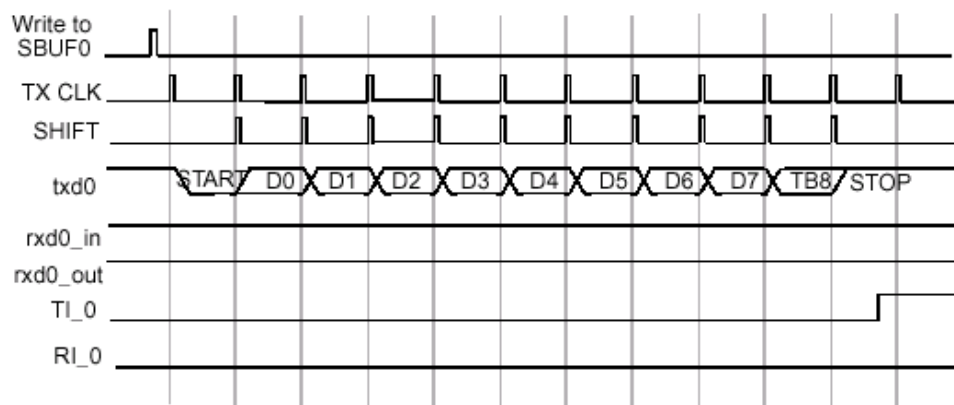


Figure 30 Serial port Mode 2 Transmit Timing.



18.9.3.2 Mode 2 Receive

Figure 31 illustrates the mode 2 receive timing. Reception begins at the falling edge of a start bit received on rxd_in, when enabled by the REN bit. For this purpose, rxd_in is sampled sixteen times per bit for any baud rate. When a falling edge of a start bit is detected, the divide-by-16 counter used to generate the receive clock is reset to align the counter rollover to the bit boundaries.

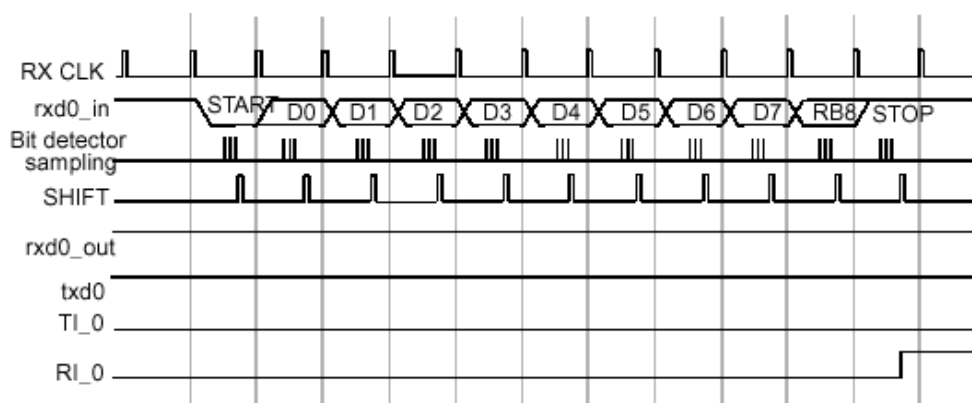


Figure 31 Serial port Mode 2 Receive Timing.

For noise rejection, the serial port establishes the content of each received bit by a majority decision of three consecutive samples in the middle of each bit time. This is especially true for the start bit. If the falling edge on rxd_in is not verified by a majority decision of three consecutive samples (low), then the serial port stops reception and waits for another falling edge on rxd_in.

At the middle of the stop bit time, the serial port checks for the following conditions:

- RI = 0
- If SM2 = 1, the state of the stop bit is 1
(if SM2 = 0, the state of the stop bit does not matter)

If the above conditions are met, the serial port then writes the received byte to the SBUF register, loads the 9th received bit into RB8, and sets the RI bit. If the above conditions are not met, the received data is lost, the SBUF register and RB8 bit are not loaded, and the RI bit is not set. After the middle of the stop bit time, the serial port waits for another high-to-low transition on the rxd_in.

18.9.4 Mode 3

Mode 3 provides asynchronous, full-duplex communication, using a total of eleven bits:

- One start bit
- Eight data bits
- One programmable 9th bit
- One stop bit; the data bits are transmitted and received LSB first

The mode 3 transmit and receive operations are identical to mode 2. The mode 3 baud rate generation is identical to mode 1. That is, mode 3 is a combination of mode 2 protocol and mode 1 baud rate. Figure 32 illustrates the mode 3 transmit timing. Mode 3 operation is identical to that of the standard 8051 when Timers 1 and 2 use CPU_clk/12 (the default).

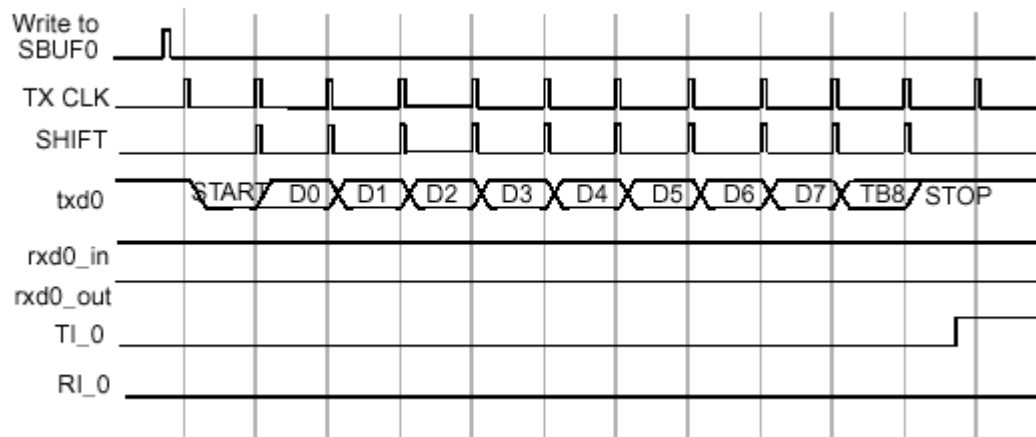


Figure 32 Serial port Mode 3 Transmit Timing.

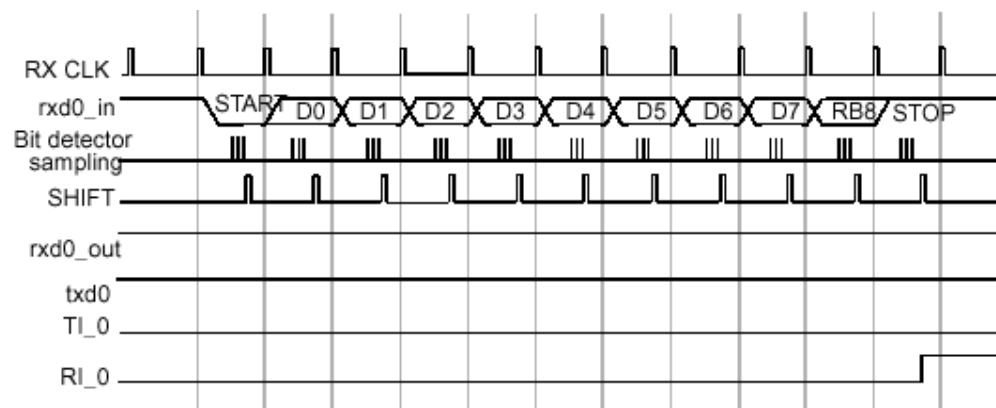


Figure 33 illustrates the mode 3 receive timing.

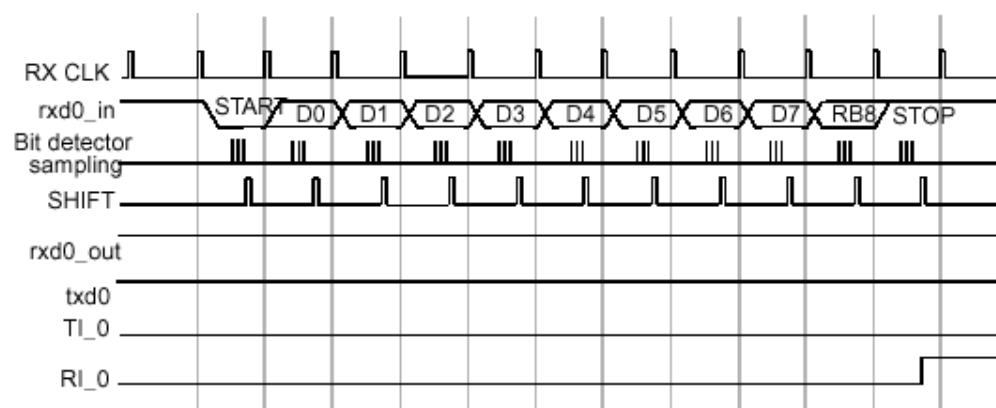


Figure 33 Serial port Mode 3 Receive Timing.



18.9.5 Multiprocessor Communications

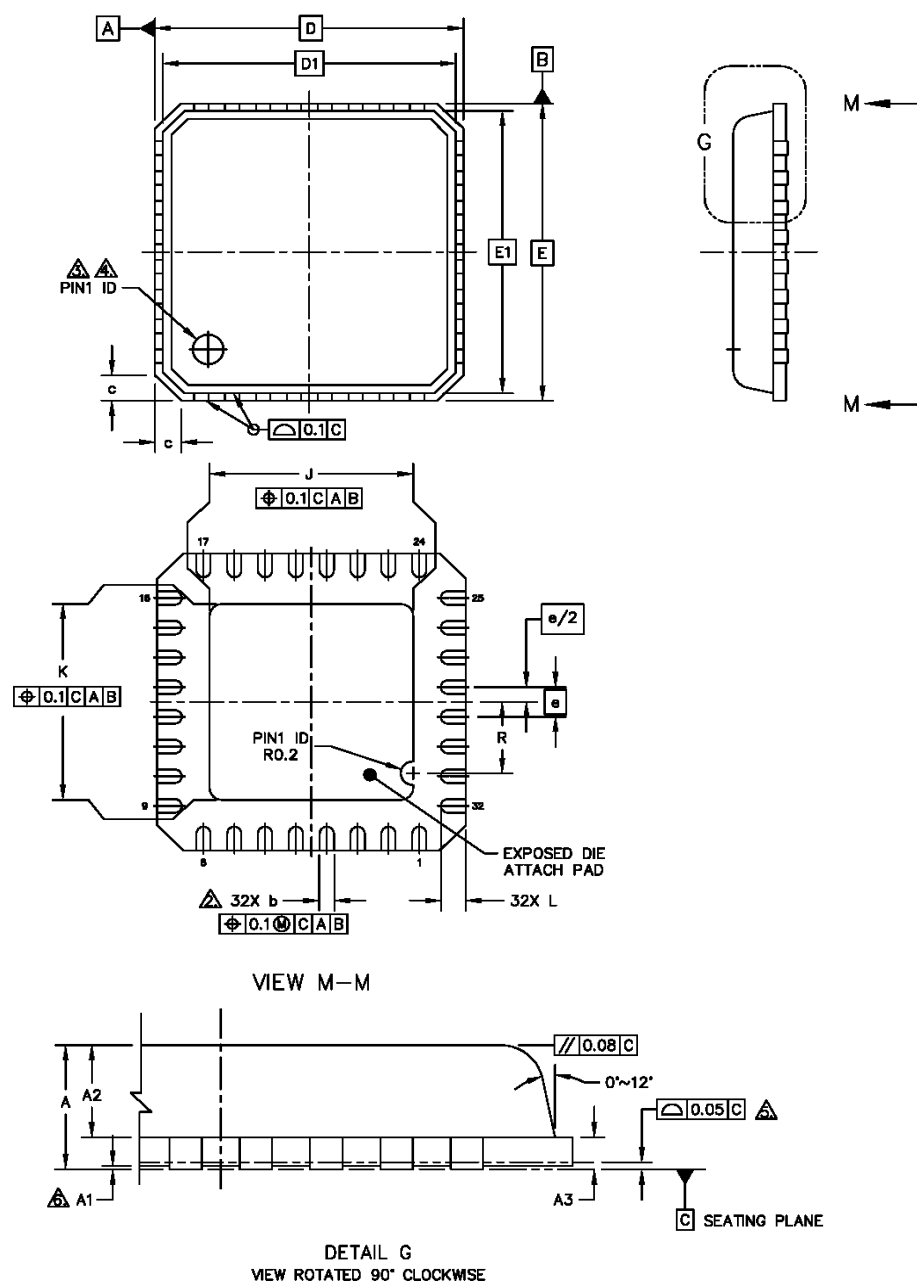
The multiprocessor communication feature is enabled in modes 2 and 3 when the SM2 bit is set in the SCON SFR for a serial port. In multiprocessor communication mode, the 9th bit received is stored in RB8 and, after the stop bit is received, the serial port interrupt is activated only if RB8 = 1. A typical use for the multiprocessor communication feature is when a master wants to send a block of data to one of several slaves. The master first transmits an address byte that identifies the target slave. When transmitting an address byte, the master sets the 9th bit to 1; for data bytes, the 9th bit is 0.

When SM2 = 1, no slave will be interrupted by a data byte. However, an address byte interrupts all slaves so that each slave can examine the received address byte to determine whether that slave is being addressed. Address decoding must be done by software during the interrupt service routine. The addressed slave clears its SM2 bit and prepares to receive the data bytes. The slaves that are not being addressed leave the SM2 bit set and ignore the incoming data bytes.



19 PACKAGE OUTLINE

nRF9E5 uses the QFN 32L 5x5 green package with a mat tin finish. Dimensions are in mm. Recommended soldering reflow profile can be found in application note nAN400-08, QFN soldering reflow guidelines, www.nvlsi.no.



Package Type		A	A1	A2	b	D	E	e	J	K	L
QFN32 (5x5 mm)	Min	0.8	0.0	0.65	0.18	5 BSC	5 BSC	0.5 BSC	3.2	3.2	0.3
	typ.				0.23				3.3	3.3	0.4
	Max	0.9	0.05	0.69	0.3				3.4	3.4	0.5

Figure 34 nRF9E5 package outline.



20 PCB LAYOUT AND DECOUPLING GUIDELINES

nRF9E5 is an extremely robust RF device due to internal voltage regulators and requires the minimum of RF layout protocols. However the following design rules should still be incorporated into the layout design.

A PCB with a minimum of two layers including a ground plane is recommended for optimum performance. The nRF9E5 DC supply voltage should be decoupled as close as possible to the VDD pins with high performance RF capacitors. It is preferable to mount a large surface mount capacitor (e.g. 4.7 μ F tantalum) in parallel with the smaller value capacitors. The nRF9E5 supply voltage should be filtered and routed separately from the supply voltages of any digital circuitry.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections and VDD bypass capacitors must be connected as close as possible to the nRF9E5 IC. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to place via holes as close as possible to the VSS pins. A minimum of one via hole should be used for each VSS pin.

Full swing digital data or control signals should not be routed close to the crystal or the power supply lines.

A fully qualified RF-layout for the nRF9E5 and its surrounding components, including antennas and matching networks, can be downloaded from www.nvlsi.no.



21 APPLICATION EXAMPLES

21.1 Differential Connection to a Loop Antenna

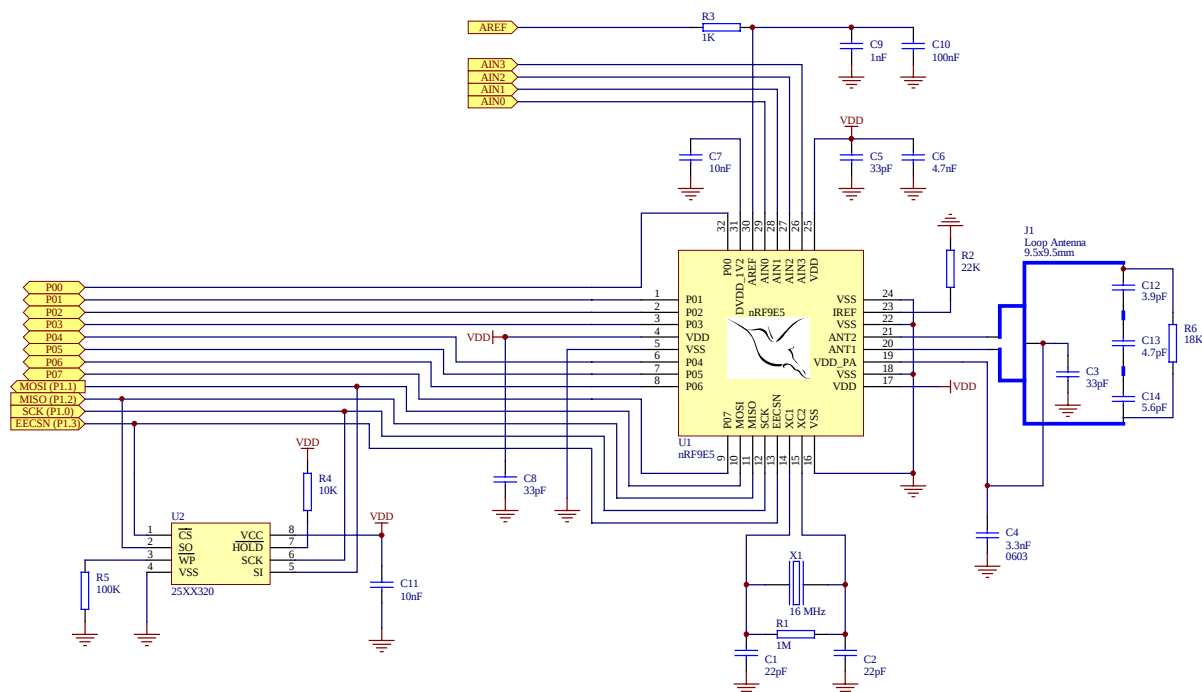


Figure 35 nRF9E5 application schematic, differential connection to a loop antenna (868MHz).



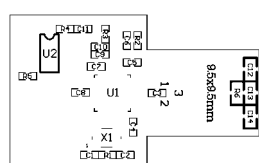
Component	Description	Size	Value	Tol.	Units
C1	NP0 ceramic chip capacitor, (Crystal oscillator)	0603	22	±5%	pF
C2	NP0 ceramic chip capacitor, (Crystal oscillator)	0603	22	±5%	pF
C3	NP0 ceramic chip capacitor, (PA supply decoupling)	0603	33	±5%	pF
C4	X7R ceramic chip capacitor, (PA supply decoupling)	0603	3.3	±10%	nF
C5	NP0 ceramic chip capacitor, (Supply decoupling)	0603	33	±5%	pF
C6	X7R ceramic chip capacitor, (Supply decoupling)	0603	4.7	±10%	nF
C7	X7R ceramic chip capacitor, (Supply decoupling)	0603	10	±10%	nF
C8	NP0 ceramic chip capacitor, (Supply decoupling)	0603	33	±5%	pF
C9	X7R ceramic chip capacitor, (AREF filtering)	0603	1	±10%	nF
C10	X7R ceramic chip capacitor, (AREF filtering)	0603	100	±10%	nF
C11	X7R ceramic chip capacitor	0603	10	±10%	nF
C12	NP0 ceramic chip capacitor, (Antenna tuning)	0603	3.9	±0.1	pF
C13	NP0 ceramic chip capacitor, (Antenna tuning)	0603	4.7	±0.1	pF
C14	NP0 ceramic chip capacitor, (Antenna tuning)	0603	5.6	±0.1	pF
R1	0.1W chip resistor, (Crystal oscillator bias)	0603	1	±1%	MΩ
R2	0.1W chip resistor, (Reference bias)	0603	22	±1%	kΩ
R3	0.1W chip resistor	0603	1	±1%	kΩ
R4	0.1W chip resistor	0603	10	±1%	kΩ
R5	0.1W chip resistor	0603	100	±1%	kΩ
R6	0.1W chip resistor, (Antenna Q reduction)	0603	18	±1%	kΩ
U1	nRF9E5 Transceiver	QFN32L/5x5			
U2	4 kbyte serial EEPROM with SPI interface	SO8	2XX320		
X1	Crystal (see chapter 7.1)	LxWxH = 4.0x2.5x0.8	16	±30ppm	MHz

Table 74 Recommended External Components, differential connection to a loop antenna (868MHz).



21.2 PCB Layout Example, Differential Connection to a Loop Antenna

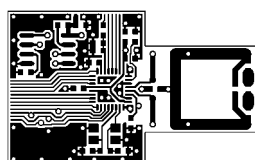
Figure 36 shows a PCB layout example for the application schematic in Figure 35. A double-sided FR-4 board of 1.6mm thickness is used. This PCB has a ground plane on the bottom layer. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. A large number of via holes connect the top layer ground areas to the bottom layer ground plane. There is no ground plane beneath the antenna.



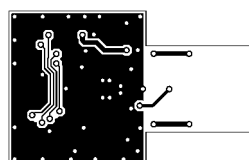
a) Top silk screen

No components in bottom layer

b) Bottom silk screen



c) Top view



d) Bottom view

Figure 36 PCB layout example for nRF9E5, differential connection to a loop antenna.



21.3 Single Ended Connection to 50Ω Antenna

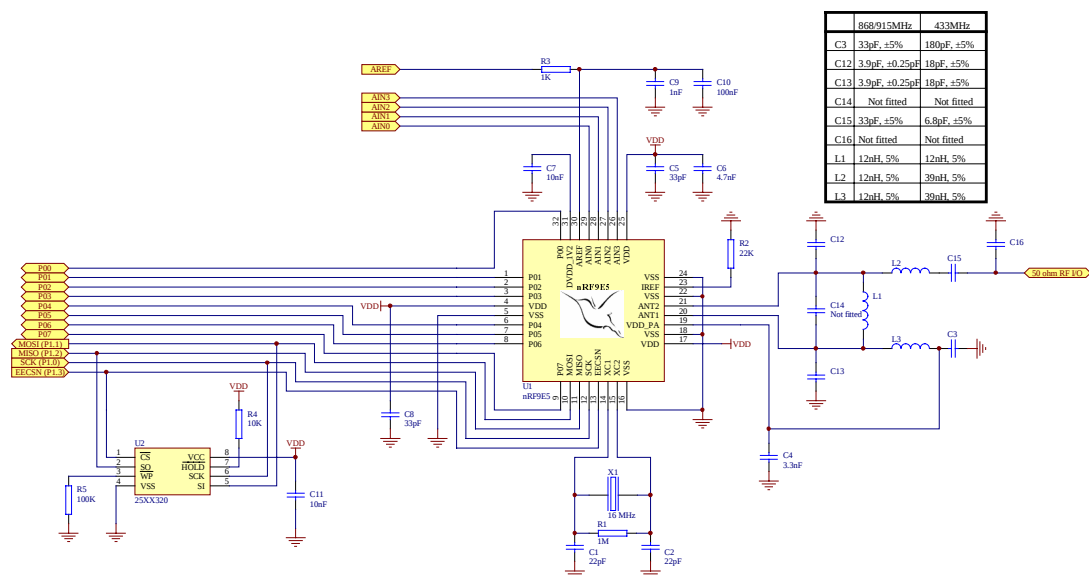


Figure 37 nRF9E5 application schematic, single ended connection to 50Ω antenna by using a differential to single ended matching network.



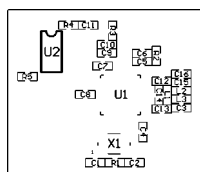
Component	Description	Size	Value	Tol.	Units
C1	NP0 ceramic chip capacitor, (Crystal oscillator)	0603	22	±5%	pF
C2	NP0 ceramic chip capacitor, (Crystal oscillator)	0603	22	±5%	pF
C3	NP0 ceramic chip capacitor, (PA supply decoupling) @ 433MHz @ 868 @ 915MHz	0603	180 33 33	±5%	pF
C4	X7R ceramic chip capacitor, (PA supply decoupling)	0603	3.3	±10%	nF
C5	NP0 ceramic chip capacitor, (Supply decoupling)	0603	33	±5%	pF
C6	X7R ceramic chip capacitor, (Supply decoupling)	0603	4.7	±10%	nF
C7	X7R ceramic chip capacitor, (Supply decoupling)	0603	10	±10%	nF
C8	NP0 ceramic chip capacitor, (Supply decoupling)	0603	33	±5%	pF
C9	X7R ceramic chip capacitor, (AREF filtering)	0603	1	±10%	nF
C10	X7R ceramic chip capacitor, (AREF filtering)	0603	100	±10%	nF
C11	X7R ceramic chip capacitor	0603	10	±10%	nF
C12	NP0 ceramic chip capacitor, (Impedance matching) @ 433MHz @ 868 @ 915MHz	0603	18 3.9 3.9	±5% <±0.25pF <±0.25pF	pF
C13	NP0 ceramic chip capacitor, (Impedance matching) @ 433MHz @ 868 @ 915MHz	0603	18 3.9 3.9	±5% <±0.25pF <±0.25pF	pF
C14	NP0 ceramic chip capacitor, (Impedance matching)	0603	Not fitted		pF
C15	NP0 ceramic chip capacitor, (Impedance matching) @ 433MHz @ 868 @ 915MHz	0603	6.8 33 33	±5% ±5% ±5%	pF
C16	NP0 ceramic chip capacitor, (Impedance matching) @ 433MHz @ 868 @ 915MHz	0603	Not fitted Not fitted Not fitted		pF
L1	Chip inductor, (Impedance matching) @ 433MHz: SRF> 433MHz @ 868MHz: SRF> 868MHz @ 915MHz: SRF> 915MHz	0603	12 12 12	±5%	nH
L2	Chip inductor, (Impedance matching) @ 433MHz: SRF> 433MHz @ 868MHz: SRF> 868MHz @ 915MHz: SRF> 915MHz	0603	39 12 12	±5% ±5% ±5%	nH
L3	Chip inductor, (Impedance matching) @ 433MHz: SRF> 433MHz @ 868MHz: SRF> 868MHz @ 915MHz: SRF> 915MHz	0603	39 12 12	±5% ±5% ±5%	nH
R1	0.1W chip resistor, (Crystal oscillator bias)	0603	1	±1%	MΩ
R2	0.1W chip resistor, (Reference bias)	0603	22	±1%	kΩ
R3	0.1W chip resistor	0603	1	±1%	kΩ
R4	0.1W chip resistor	0603	10	±1%	kΩ
R5	0.1W chip resistor	0603	100	±1%	kΩ
U1	nRF9E5 Transceiver	QFN32L/5x5			
U2	4 kbyte serial EEPROM with SPI interface	SO8	2XX320		
X1	Crystal (see chapter 7.1)	LxWxH = 4.0x2.5x0.8	16	±30ppm	MHz

Table 75 Recommended External Components, single ended connection to 50Ω antenna.



21.4 PCB Layout Example, Single Ended Connection to 50Ω Antenna

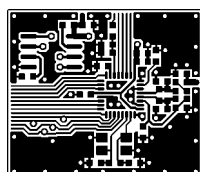
Figure 38 shows a PCB layout example for the application schematic in Figure 37. A double-sided FR-4 board of 1.6mm thickness is used. This PCB has a ground plane on the bottom layer. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. A large number of via holes connect the top layer ground areas to the bottom layer ground plane.



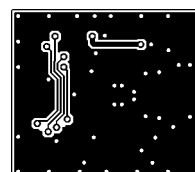
a) Top silk screen

No components in bottom layer

b) Bottom silk screen



c) Top view



d) Bottom view

Figure 38 PCB layout example for nRF9E5, single ended connection to 50Ω antenna by using a differential to single ended matching network.

21.5 Configure the Chip as nRF905.

nRF9E5 is easily configurable as nRF905. Upon power up the boot loader is run. If MISO is set to low value during the first 10ms, the microcontroller configures itself to nRF905 mode. All pins are then defined as for the nRF905 chip.



22 ABSOLUTE MAXIMUM RATINGS

Supply Voltage

VDD - 0.3V to + 3.6V

VSS 0V

Input Voltage

V_I - 0.3V to VDD + 0.3V

Output Voltage

V_O - 0.3V to VDD + 0.3V

Total Power Dissipation

P_D (T_A=85°C).....230mW

Temperatures

Operating temperature..... - 40°C to + 85°C

Storage temperature.....- 40°C to + 125°C

Note: Stress exceeding one or more of the limiting values may cause permanent damage to the device.

ATTENTION!

Electrostatic sensitive device.

Observe precaution for handling.





23 GLOSSARY OF TERMS

Term	Description
ADC	Analog to Digital Converter
AM	Address Match
BOM	Bill Of Material
CD	Carrier Detect
CLK	Clock
CRC	Cyclic Redundancy Check
CSN	SPI Chip Select Not
DR	Data Ready
GFSK	Gaussian Frequency Shift Keying
GPIO	General Purpose Input Output
ISM	Industrial-Scientific-Medical
ksps	kilo Samples per Second
MCU	Micro Controller Unit
MISO	SPI Master In Slave Out
MOSI	SPI Master Out Slave In
PWM	Pulse-Width Modulation
PWR_DWN	Power Down
PWR_UP	Power Up
RAM	Random Access Memory
ROM	Read Only Memory
RTC	Real Time Clock
RX	Receive
SCK	SPI Serial Clock
SPI	Serial Programmable Interface
STBY	Standby
TRX_EN	Transmit/Receive Enable
TX	Transmit
TX_EN	Transmit Enable
UART	Universal Asynchronous Receiver Transmitter
XTAL	Crystal

Table 76 Glossary of terms.



24 DEFINITIONS

Data sheet status	
Objective product specification	This datasheet contains target specifications for product development.
Preliminary product specification	This datasheet contains preliminary data; supplementary data may be published from Nordic VLSI ASA later.
Product specification	This datasheet contains final product specifications. Nordic VLSI ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Limiting values	
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Table 77 Definitions.

Nordic VLSI ASA reserves the right to make changes without further notice to the product to improve reliability, function or design. Nordic VLSI does not assume any liability arising out of the application or use of any product or circuits described herein.

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Nordic VLSI ASA customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nordic VLSI ASA for any damages resulting from such improper use or sale.

Product specification revision date: 29.01.2004

Datasheet order code: 290104nRF9E5

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25 YOUR NOTES



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