MSP430x22x2, MSP430x22x4
MIXED SIGNAL MICROCONTROLLER

SLAS504C – JULY 2006 – REVISED MAY 2009

- **Low Supply Voltage Range: 1.8 V to 3.6 V**
- **Ultralow Power Consumption**
  - **Active Mode: 270 μA at 1 MHz, 2.2 V**
  - **Standby Mode: 0.7 μA**
  - **Off Mode (RAM Retention): 0.1 μA**
- **Ultrafast Wake-Up From Standby Mode in Less Than 1 μs**
- **16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time**
- **Basic Clock Module Configurations:**
  - **Internal Frequencies up to 16 MHz With Four Calibrated Frequencies to ±1%**
  - **Internal Very-Low-Power Low-Frequency Oscillator**
  - **32-kHz Crystal**
  - **High-Frequency Crystal up to 16 MHz**
  - **Resonator**
  - **External Digital Clock Source**
  - **External Resistor**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **16-Bit Timer_B With Three Capture/Compare Registers**
- **Universal Serial Communication Interface**
  - **Enhanced UART Supporting Auto-Baudrate Detection (LIN)**
  - **IrDA Encoder and Decoder**
  - **Synchronous SPI**
  - **I^2C™**
- **10-Bit 200-ksps Analog-to-Digital (A/D) Converter With Internal Reference, Sample-and-Hold, Autoscan, and Data Transfer Controller**
- **Two Configurable Operational Amplifiers (MSP430x22x4 Only)**
- **Brownout Detector**
- **Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse**
- **Bootstrap Loader**
- **On Chip Emulation Module**
- **Family Members Include:**
  MSP430F2232: 8KB + 256B Flash Memory
  512B RAM
  MSP430F2252: 16KB + 256B Flash Memory
  512B RAM
  MSP430F2272: 32KB + 256B Flash Memory
  1KB RAM
  MSP430F2234: 8KB + 256B Flash Memory
  512B RAM
  MSP430F2254: 16KB + 256B Flash Memory
  512B RAM
  MSP430F2274: 32KB + 256B Flash Memory
  1KB RAM
- **Available in a 38-Pin Thin Shrink Small-Outline Package (TSSOP) (DA) and 40-Pin QFN Package (RHA) (See Available Options)**
- **For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide*, Literature Number SLAU144**

description

The Texas Instruments MSP430 family of ultralow-power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 μs.

description (continued)

The MSP430x22xx series is an ultralow-power mixed signal microcontroller with two built-in 16-bit timers, a universal serial communication interface, 10-bit A/D converter with integrated reference and data transfer controller (DTC), two general-purpose operational amplifiers in the MSP430x22x4 devices, and 32 I/O pins.

Typical applications include sensor systems that capture analog signals, convert them to digital values, and then process the data for display or for transmission to a host system. Stand-alone radio-frequency (RF) sensor front ends are another area of application.

AVAILABLE OPTIONS†

T_A	PACKAGED DEVICES‡	
	PLASTIC 38-PIN TSSOP (DA)	PLASTIC 40-PIN QFN (RHA)
−40°C to 85°C	MSP430F2232IDA MSP430F2252IDA MSP430F2272IDA MSP430F2234IDA MSP430F2254IDA MSP430F2274IDA	MSP430F2232IRHA MSP430F2252IRHA MSP430F2272IRHA MSP430F2234IRHA MSP430F2254IRHA MSP430F2274IRHA
−40°C to 105°C	MSP430F2232TDA§ MSP430F2252TDA§ MSP430F2272TDA§ MSP430F2234TDA MSP430F2254TDA MSP430F2274TDA	MSP430F2232TRHA§ MSP430F2252TRHA§ MSP430F2272TRHA§ MSP430F2234TRHA MSP430F2254TRHA MSP430F2274TRHA

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
‡ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
§ Product Preview

DEVELOPMENT TOOL SUPPORT

All MSP430 microcontrollers include an Embedded Emulation Module (EEM) allowing advanced debugging and programming through easy to use development tools. Recommended hardware options include the following:

- Debugging and Programming Interface
  - MSP-FET430UIF (USB)
  - MSP-FET430PIF (Parallel Port)
- Debugging and Programming Interface with Target Board
  - MSP-FET430U38 (DA package)
- Production Programmer
  - MSP-GANG430

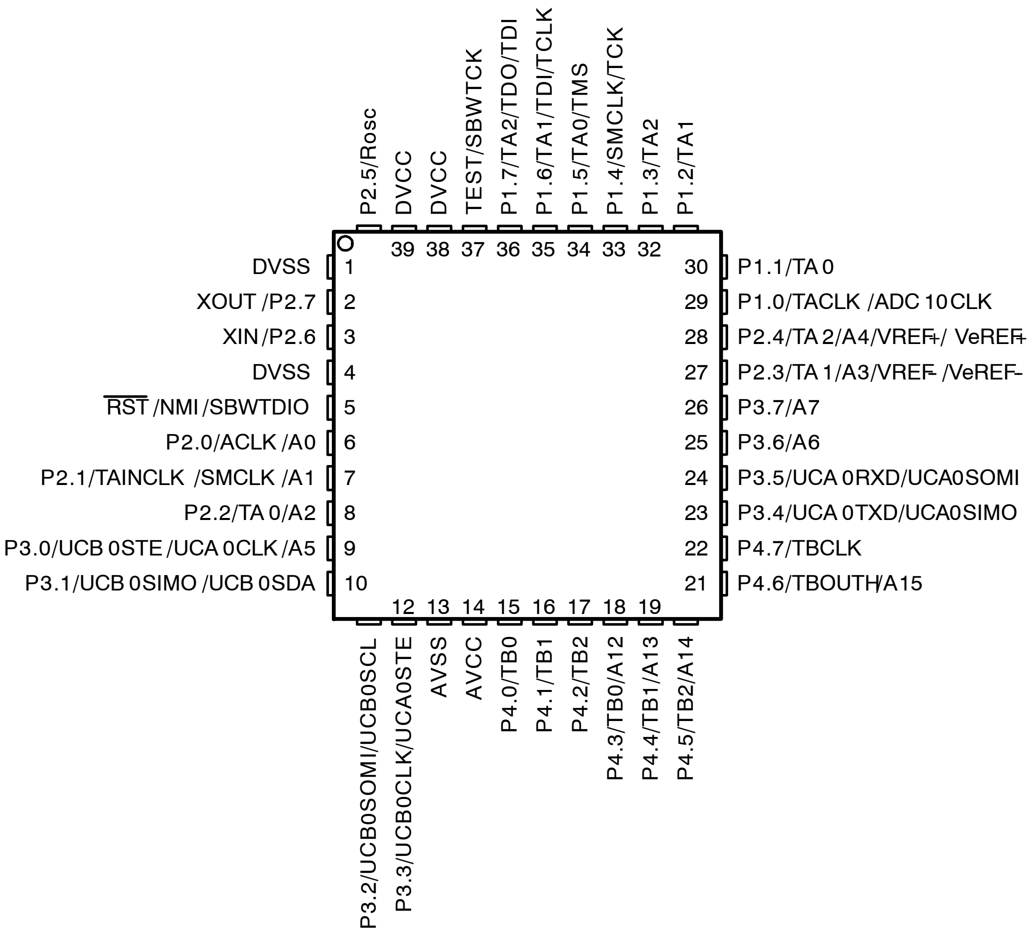
MSP430x22x2 device pinout, DA package

TEST/SBWTCK	1	38	P1.7/TA2/TDO/TDI
DVCC	2	37	P1.6/TA1/TDI
P2.5/Rosc	3	36	P1.5/TA0/TMS
DVSS	4	35	P1.4/SMCLK/TCK
XOUT/P2.7	5	34	P1.3/TA2
XIN/P2.6	6	33	P1.2/TA1
$\overline{\text{RST}}$/NMI/SBWTDIO	7	32	P1.1/TA0
P2.0/ACLK/A0	8	31	P1.0/TACLK/ADC10CLK
P2.1/TAINCLK/SMCLK/A1	9	30	P2.4/TA2/A4/VREF+/VeREF+
P2.2/TA0/A2	10	29	P2.3/TA1/A3/VREF−/VeREF−
P3.0/UCB0STE/UCA0CLK/A5	11	28	P3.7/A7
P3.1/UCB0SIMO/UCB0SDA	12	27	P3.6/A6
P3.2/UCB0SOMI/UCB0SCL	13	26	P3.5/UCA0RXD/UCA0SOMI
P3.3/UCB0CLK/UCA0STE	14	25	P3.4/UCA0TXD/UCA0SIMO
AVSS	15	24	P4.7/TBCLK
AVCC	16	23	P4.6/TBOUTH/A15
P4.0/TB0	17	22	P4.5/TB2/A14
P4.1/TB1	18	21	P4.4/TB1/A13
P4.2/TB2	19	20	P4.3/TB0/A12

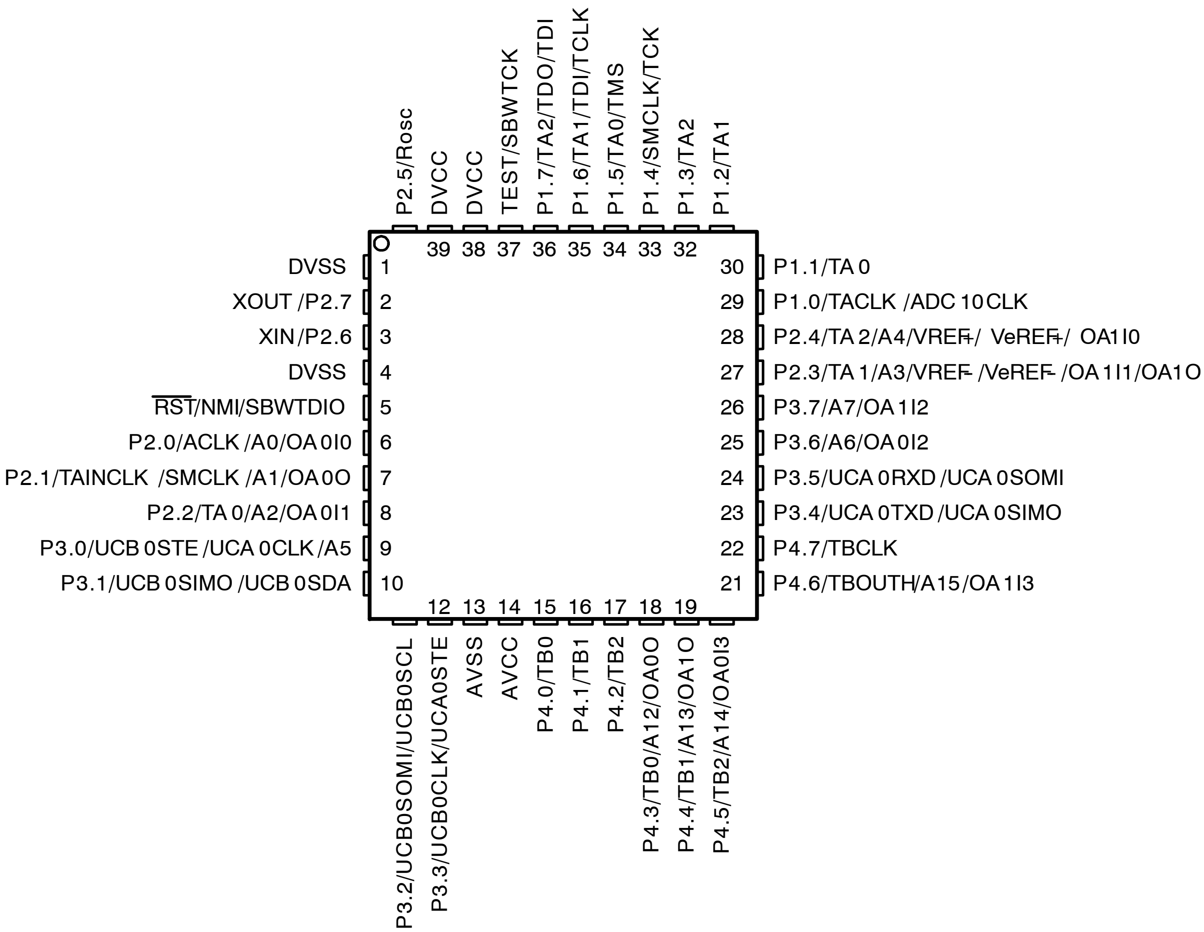
MSP430x22x4 device pinout, DA package

TEST/SBWTCK	1	38	P1.7/TA2/TDO/TDI
DVCC	2	37	P1.6/TA1/TDI
P2.5/Rosc	3	36	P1.5/TA0/TMS
DVSS	4	35	P1.4/SMCLK/TCK
XOUT/P2.7	5	34	P1.3/TA2
XIN/P2.6	6	33	P1.2/TA1
$\overline{\text{RST}}$/NMI/SBWTDIO	7	32	P1.1/TA0
P2.0/ACLK/A0/OA0I0	8	31	P1.0/TACLK/ADC10CLK
P2.1/TAINCLK/SMCLK/A1/OA0O	9	30	P2.4/TA2/A4/VREF+/VeREF+/OA1I0
P2.2/TA0/A2/OA0I1	10	29	P2.3/TA1/A3/VREF−/VeREF−/OA1I1/OA1O
P3.0/UCB0STE/UCA0CLK/A5	11	28	P3.7/A7/OA1I2
P3.1/UCB0SIMO/UCB0SDA	12	27	P3.6/A6/OA0I2
P3.2/UCB0SOMI/UCB0SCL	13	26	P3.5/UCA0RXD/UCA0SOMI
P3.3/UCB0CLK/UCA0STE	14	25	P3.4/UCA0TXD/UCA0SIMO
AVSS	15	24	P4.7/TBCLK
AVCC	16	23	P4.6/TBOUTH/A15/OA1I3
P4.0/TB0	17	22	P4.5/TB2/A14/OA0I3
P4.1/TB1	18	21	P4.4/TB1/A13/OA1O
P4.2/TB2	19	20	P4.3/TB0/A12/OA0O

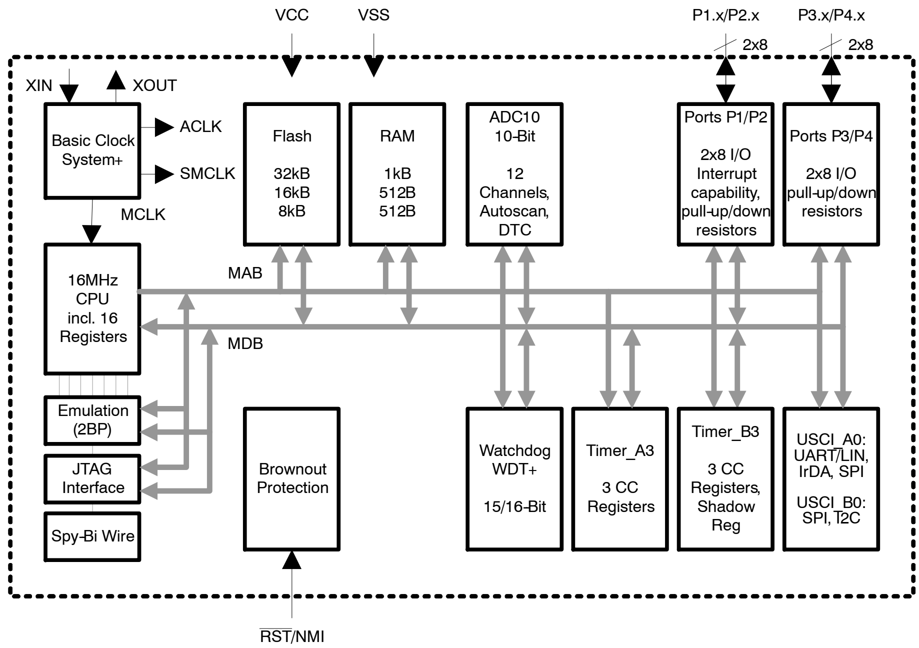
MSP430x22x2 device pinout, RHA package



MSP430x22x4 device pinout, RHA package

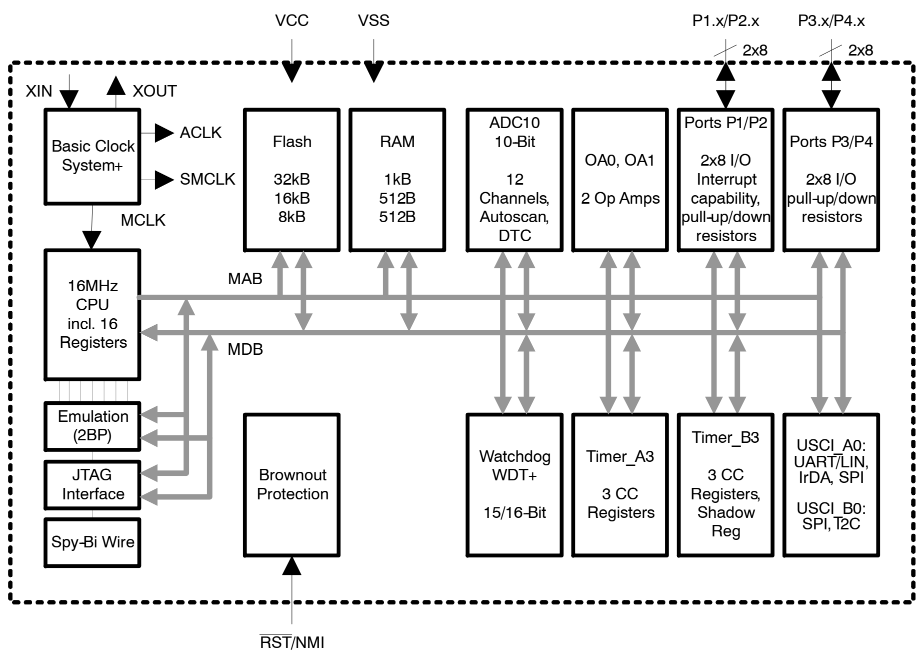


MSP430x22x2 functional block diagram



NOTE: See port schematics section for detailed I/O information.

MSP430x22x4 functional block diagram



NOTE: See port schematics section for detailed I/O information.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Terminal Functions, MSP430x22x2

TERMINAL				DESCRIPTION
NAME	DA NO.	RHA NO.	I/O	
P1.0/TACLK/ ADC10CLK	31	29	I/O	General-purpose digital I/O pin Timer_A, clock signal TACLK input ADC10, conversion clock
P1.1/TA0	32	30	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: OUT0 output/BSL transmit
P1.2/TA1	33	31	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1A input, compare: OUT1 output
P1.3/TA2	34	32	I/O	General-purpose digital I/O pin Timer_A, capture: CCI2A input, compare: OUT2 output
P1.4/SMCLK/ TCK	35	33	I/O	General-purpose digital I/O pin / SMCLK signal output Test Clock input for device programming and test
P1.5/TA0/ TMS	36	34	I/O	General-purpose digital I/O pin / Timer_A, compare: OUT0 output Test Mode Select input for device programming and test
P1.6/TA1/ TDI/TCLK	37	35	I/O	General-purpose digital I/O pin / Timer_A, compare: OUT1 output Test Data Input or Test Clock Input for programming and test
P1.7/TA2/ TDO/TDI†	38	36	I/O	General-purpose digital I/O pin / Timer_A, compare: OUT2 output Test Data Output or Test Data Input for programming and test
P2.0/ACLK/A0	8	6	I/O	General-purpose digital I/O pin / ACLK output ADC10, analog input A0
P2.1/TAINCLK/SMCLK/A1	9	7	I/O	General-purpose digital I/O pin Timer_A, clock signal at INCLK, SMCLK signal output ADC10, analog input A1
P2.2/TA0/A2	10	8	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0B input/BSL receive, compare: OUT0 output ADC10, analog input A2
P2.3/TA1/ A3/V_{REF-}/V_{eREF-}	29	27	I/O	General-purpose digital I/O pin Timer_A, capture CCI1B input, compare: OUT1 output ADC10, analog input A3 / negative reference voltage output/input
P2.4/TA2/ A4/V_{REF+}/V_{eREF+}	30	28	I/O	General-purpose digital I/O pin / Timer_A, compare: OUT2 output ADC10, analog input A4 / positive reference voltage output/input
P2.5/ R_{OSC}	3	40	I/O	General-purpose digital I/O pin Input for external DCO resistor to define DCO frequency
XIN/P2.6	6	3	I/O	Input terminal of crystal oscillator General-purpose digital I/O pin
XOUT/P2.7	5	2	I/O	Output terminal of crystal oscillator General-purpose digital I/O pin
P3.0/ UCB0STE/UCA0CLK/ A5	11	9	I/O	General-purpose digital I/O pin USCI_B0 slave transmit enable / USCI_A0 clock input/output ADC10, analog input A5
P3.1/ UCB0SIMO/UCB0SDA	12	10	I/O	General-purpose digital I/O pin USCI_B0 slave in/master out in SPI mode, SDA I^2C data in I^2C mode
P3.2/ UCB0SOMI/UCB0SCL	13	11	I/O	General-purpose digital I/O pin USCI_B0 slave out/master in in SPI mode, SCL I^2C clock in I^2C mode
P3.3/ UCB0CLK/UCA0STE	14	12	I/O	General-purpose digital I/O pin USCI_B0 clock input/output / USCI_A0 slave transmit enable
P3.4/ UCA0TXD/UCA0SIMO	25	23	I/O	General-purpose digital I/O pin USCI_A0 transmit data output in UART mode, slave in/master out in SPI mode

Terminal Functions, MSP430x22x2 (Continued)

TERMINAL				DESCRIPTION
NAME	DA NO.	RHA NO.	I/O	
P3.5/ UCA0RXD/UCA0SOMI	26	24	I/O	General-purpose digital I/O pin USCI_A0 receive data input in UART mode, slave out/master in in SPI mode
P3.6/A6	27	25	I/O	General-purpose digital I/O pin ADC10 analog input A6
P3.7/A7	28	26	I/O	General-purpose digital I/O pin ADC10 analog input A7
P4.0/TB0	17	15	I/O	General-purpose digital I/O pin Timer_B, capture: CCI0A input, compare: OUT0 output
P4.1/TB1	18	16	I/O	General-purpose digital I/O pin Timer_B, capture: CCI1A input, compare: OUT1 output
P4.2/TB2	19	17	I/O	General-purpose digital I/O pin Timer_B, capture: CCI2A input, compare: OUT2 output
P4.3/TB0/ A12	20	18	I/O	General-purpose digital I/O pin Timer_B, capture: CCI0B input, compare: OUT0 output ADC10 analog input A12
P4.4/TB1 A13	21	19	I/O	General-purpose digital I/O pin Timer_B, capture: CCI1B input, compare: OUT1 output ADC10 analog input A13
P4.5/TB2 A14	22	20	I/O	General-purpose digital I/O pin Timer_B, compare: OUT2 output ADC10 analog input A14
P4.6/TBOUTH A15	23	21	I/O	General-purpose digital I/O pin Timer_B, switch all TB0 to TB3 outputs to high impedance ADC10 analog input A15
P4.7/TBCLK	24	22	I/O	General-purpose digital I/O pin Timer_B, clock signal TBCLK input
$\overline{\text{RST}}$/NMI/SBWTDIO	7	5	I	Reset or nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/SBWTCK	1	37	I	Selects test mode for JTAG pins on Port1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test
DV_{CC}	2	38, 39		Digital supply voltage
AV_{CC}	16	14		Analog supply voltage
DV_{SS}	4	1, 4		Digital ground reference
AV_{SS}	15	13		Analog ground reference
QFN Pad	NA	Package Pad	NA	QFN package pad; connection to DV_{SS} recommended.

† TDO or TDI is selected via JTAG instruction.

NOTE: If XOUT/P2.7/CA7 is used as an input, excess current will flow until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

Terminal Functions, MSP430x22x4

TERMINAL NAME	DA NO.	RHA NO.	I/O	DESCRIPTION
P1.0/TACLK/ ADC10CLK	31	29	I/O	General-purpose digital I/O pin Timer_A, clock signal TACLK input ADC10, conversion clock
P1.1/TA0	32	30	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: OUT0 output/BSL transmit
P1.2/TA1	33	31	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1A input, compare: OUT1 output
P1.3/TA2	34	32	I/O	General-purpose digital I/O pin Timer_A, capture: CCI2A input, compare: OUT2 output
P1.4/SMCLK/ TCK	35	33	I/O	General-purpose digital I/O pin / SMCLK signal output Test Clock input for device programming and test
P1.5/TA0/ TMS	36	34	I/O	General-purpose digital I/O pin / Timer_A, compare: OUT0 output Test Mode Select input for device programming and test
P1.6/TA1/ TDI/TCLK	37	35	I/O	General-purpose digital I/O pin / Timer_A, compare: OUT1 output Test Data Input or Test Clock Input for programming and test
P1.7/TA2/ TDO/TDI†	38	36	I/O	General-purpose digital I/O pin / Timer_A, compare: OUT2 output Test Data Output or Test Data Input for programming and test
P2.0/ACLK/A0/OA0I0	8	6	I/O	General-purpose digital I/O pin / ACLK output ADC10, analog input A0 / OA0, analog input I0
P2.1/TAINCLK/SMCLK/ A1/OA0O	9	7	I/O	General-purpose digital I/O pin / Timer_A, clock signal at INCLK SMCLK signal output ADC10, analog input A1 / OA0, analog output
P2.2/TA0/ A2/OA0I1	10	8	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0B input/BSL receive, compare: OUT0 output ADC10, analog input A2 / OA0, analog input I1
P2.3/TA1/ A3/V_{REF-}/V_{eREF-} /OA1I1/OA1O	29	27	I/O	General-purpose digital I/O pin Timer_A, capture CCI1B input, compare: OUT1 output ADC10, analog input A3 / negative reference voltage output/input OA1, analog input I1 / OA1, analog output
P2.4/TA2/ A4/V_{REF+}/V_{eREF+} /OA1I0	30	28	I/O	General-purpose digital I/O pin / Timer_A, compare: OUT2 output ADC10, analog input A4 / positive reference voltage output/input OA1, analog input I0
P2.5/ R_{OSC}	3	40	I/O	General-purpose digital I/O pin Input for external DCO resistor to define DCO frequency
XIN/P2.6	6	3	I/O	Input terminal of crystal oscillator General-purpose digital I/O pin
XOUT/P2.7	5	2	I/O	Output terminal of crystal oscillator General-purpose digital I/O pin
P3.0/ UCB0STE/UCA0CLK/ A5	11	9	I/O	General-purpose digital I/O pin USCI_B0 slave transmit enable / USCI_A0 clock input/output ADC10, analog input A5
P3.1/ UCB0SIMO/UCB0SDA	12	10	I/O	General-purpose digital I/O pin USCI_B0 slave in/master out in SPI mode, SDA I^2C data in I^2C mode
P3.2/ UCB01SOMI/UCB0SCL	13	11	I/O	General-purpose digital I/O pin USCI_B0 slave out/master in in SPI mode, SCL I^2C clock in I^2C mode
P3.3/ UCB0CLK/UCA0STE	14	12	I/O	General-purpose digital I/O pin USCI_B0 clock input/output / USCI_A0 slave transmit enable
P3.4/ UCA0TXD/UCA0SIMO	25	23	I/O	General-purpose digital I/O pin USCI_A0 transmit data output in UART mode, slave in/master out in SPI mode

Terminal Functions, MSP430x22x4 (Continued)

TERMINAL NAME	DA NO.	RHA NO.	I/O	DESCRIPTION
P3.5/ UCA0RXD/UCA0SOMI	26	24	I/O	General-purpose digital I/O pin USCI_A0 receive data input in UART mode, slave out/master in in SPI mode
P3.6/A6/OA0I2	27	25	I/O	General-purpose digital I/O pin ADC10 analog input A6 / OA0 analog input I2
P3.7/A7/OA1I2	28	26	I/O	General-purpose digital I/O pin ADC10 analog input A7 / OA1 analog input I2
P4.0/TB0	17	15	I/O	General-purpose digital I/O pin Timer_B, capture: CCI0A input, compare: OUT0 output
P4.1/TB1	18	16	I/O	General-purpose digital I/O pin Timer_B, capture: CCI1A input, compare: OUT1 output
P4.2/TB2	19	17	I/O	General-purpose digital I/O pin Timer_B, capture: CCI2A input, compare: OUT2 output
P4.3/TB0/ A12/OA0O	20	18	I/O	General-purpose digital I/O pin Timer_B, capture: CCI0B input, compare: OUT0 output ADC10 analog input A12 / OA0 analog output
P4.4/TB1 A13/OA1O	21	19	I/O	General-purpose digital I/O pin Timer_B, capture: CCI1B input, compare: OUT1 output ADC10 analog input A13 / OA1 analog output
P4.5/TB2 A14/OA0I3	22	20	I/O	General-purpose digital I/O pin Timer_B, compare: OUT2 output ADC10 analog input A14 / OA0 analog input I3
P4.6/TBOUTH A15/OA1I3	23	21	I/O	General-purpose digital I/O pin Timer_B, switch all TB0 to TB3 outputs to high impedance ADC10 analog input A15 / OA1 analog input I3
P4.7/TBCLK	24	22	I/O	General-purpose digital I/O pin Timer_B, clock signal TBCLK input
$\overline{RST}$/NMI/SBWTDIO	7	5	I	Reset or nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/SBWTCK	1	37	I	Selects test mode for JTAG pins on Port1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test
DV_{CC}	2	38, 39		Digital supply voltage
AV_{CC}	16	14		Analog supply voltage
DV_{SS}	4	1, 4		Digital ground reference
AV_{SS}	15	13		Analog ground reference
QFN Pad	NA	Package Pad	NA	QFN package pad connection to DV_{SS} recommended.

† TDO or TDI is selected via JTAG instruction.

NOTE: If XOUT/P2.7/CA7 is used as an input, excess current will flow until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

short-form description

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

Program Counter	PC/R0
Stack Pointer	SP/R1
Status Register	SR/CG1/R2
Constant Generator	CG2/R3
General-Purpose Register	R4
General-Purpose Register	R5
General-Purpose Register	R6
General-Purpose Register	R7
General-Purpose Register	R8
General-Purpose Register	R9
General-Purpose Register	R10
General-Purpose Register	R11
General-Purpose Register	R12
General-Purpose Register	R13
General-Purpose Register	R14
General-Purpose Register	R15

instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g., ADD R4,R5	R4 + R5 ---> R5
Single operands, destination only	e.g., CALL R8	PC --> (TOS), R8--> PC
Relative jump, un/conditional	e.g., JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs,Rd	MOV R10,R11	R10 --> R11
Indexed	●	●	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)--> M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE,TONI		M(EDE) --> M(TONI)
Absolute	●	●	MOV &MEM,&TCDAT		M(MEM) --> M(TCDAT)
Indirect	●		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) --> M(Tab+R6)
Indirect autoincrement	●		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) --> R11 R10 + 2--> R10
Immediate	●		MOV #X,TONI	MOV #45,TONI	#45 --> M(TONI)

NOTE: S = source D = destination

operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active
  - MCLK is disabled
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK and SMCLK remain active
  - MCLK is disabled
  - DCO's dc-generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator is disabled
  - Crystal oscillator is stopped

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range of 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (e.g., flash is not programmed) the CPU goes into LPM4 immediately after power up.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External reset Watchdog Flash key violation PC out-of-range (see Note 1)	PORIFG RSTIFG WDTIFG KEYV (see Note 2)	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG (see Notes 2 & 4)	(non)-maskable, (non)-maskable, (non)-maskable	0FFFCh	30
Timer_B3	TBCCR0 CCIFG (see Note 3)	maskable	0FFFAh	29
Timer_B3	TBCCR1 and TBCCR2 CCIFGs, TBIFG (see Notes 2 and 3)	maskable	0FFF8h	28
			0FFF6h	27
Watchdog Timer	WDTIFG	maskable	0FFF4h	26
Timer_A3	TACCR0 CCIFG (see Note 3)	maskable	0FFF2h	25
Timer_A3	TACCR1 CCIFG. TACCR2 CCIFG TAIFG (see Notes 2 and 3)	maskable	0FFF0h	24
USCI_A0/USCI_B0 Receive	UCA0RXIFG, UCB0RXIFG (see Notes 2)	maskable	0FFEEh	23
USCI_A0/USCI_B0 Transmit	UCA0TXIFG, UCB0TXIFG (see Notes 2)	maskable	0FFECh	22
ADC10	ADC10IFG (see Note 3)	maskable	0FFEAh	21
			0FFE8h	20
I/O Port P2 (eight flags)	P2IFG.0 to P2IFG.7 (see Notes 2 and 3)	maskable	0FFE6h	19
I/O Port P1 (eight flags)	P1IFG.0 to P1IFG.7 (see Notes 2 and 3)	maskable	0FFE4h	18
			0FFE2h	17
			0FFE0h	16
(see Note 5)			0FFDEh	15
(see Note 6)			0FFDCh ... 0FFC0h	14 ... 0, lowest

NOTES:
1. A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.
2. Multiple source flags
3. Interrupt flags are located in the module.
4. (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot. Nonmaskable: neither the individual nor the general interrupt-enable bit will disable an interrupt event.
5. This location is used as bootstrap loader security key (BSLSKEY). A 0AA55h at this location disables the BSL completely. A zero (0h) disables the erasure of the flash if an invalid password is supplied.
6. The interrupt vectors at addresses 0FFDCh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

special function registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
00h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

WDTIE	Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.
OFIE	Oscillator fault enable
NMIIE	(Non)-maskable interrupt enable
ACCVIE	Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h					UCB0TXIE	UCB0RXIE	UCA0TXIE	UCA0RXIE
					rw-0	rw-0	rw-0	rw-0

UCA0RXIE	USCI_A0 receive-interrupt enable
UCA0TXIE	USCI_A0 transmit-interrupt enable
UCB0RXIE	USCI_B0 receive-interrupt enable
UCB0TXIE	USCI_B0 transmit-interrupt enable

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG
				rw−0	rw−(0)	rw−(1)	rw−1	rw−(0)

WDTIFG — Set on Watchdog Timer overflow (in watchdog mode) or security key violation.
Reset on V_{CC} power up or a reset condition at $\overline{RST}$/NMI pin in reset mode.

OFIFG — Flag set on oscillator fault

RSTIFG — External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power up.

PORIFG — Power-On interrupt flag. Set on V_{CC} power up.

NMIIFG — Set via $\overline{RST}$/NMI-pin

Address	7	6	5	4	3	2	1	0
03h					UCB0 TXIFG	UCB0 RXIFG	UCA0 TXIFG	UCA0 RXIFG
					rw−1	rw−0	rw−1	rw−0

UCA0RXIFG — USCI_A0 receive-interrupt flag

UCA0TXIFG — USCI_A0 transmit-interrupt flag

UCB0RXIFG — USCI_B0 receive-interrupt flag

UCB0TXIFG — USCI_B0 transmit-interrupt flag

Legend

rw:	Bit can be read and written.
rw-0,1:	Bit can be read and written. It is reset or set by PUC.
rw-(0,1):	Bit can be read and written. It is reset or set by POR.
(shaded box)	SFR bit is not present in device.

memory organization

		MSP430F223x	MSP430F225x	MSP430F227x
Memory	Size	8KB Flash	16KB Flash	32KB Flash
Main: interrupt vector	Flash	0FFFFh−0FFC0h	0FFFFh−0FFC0h	0FFFFh−0FFC0h
Main: code memory	Flash	0FFFFh−0E000h	0FFFFh−0C000h	0FFFFh−08000h
Information memory	Size	256 Byte	256 Byte	256 Byte
	Flash	010FFh−01000h	010FFh−01000h	010FFh−01000h
Boot memory	Size	1KB	1KB	1KB
	ROM	0FFFh−0C00h	0FFFh−0C00h	0FFFh−0C00h
RAM	Size	512 Byte	512 Byte	1KB
		03FFh−0200h	03FFh−0200h	05FFh−0200h
Peripherals	16-bit	01FFh−0100h	01FFh−0100h	01FFh−0100h
	8-bit	0FFh−010h	0FFh−010h	0FFh−010h
	8-bit SFR	0Fh−00h	0Fh−00h	0Fh−00h

bootstrap loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the *MSP430 Memory Programming User's Guide*, literature number SLAU265.

BSL FUNCTION	DA PACKAGE PINS	RHA PACKAGE PINS
Data transmit	32 - P1.1	30 - P1.1
Data receive	10 - P2.2	8 - P2.2

flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n.
  Segments A to D are also called *information memory.*
- Segment A contains calibration data. After reset, segment A is protected against programming or erasing. It can be unlocked, but care should be taken not to erase this segment if the calibration data is required.

peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, refer to the *MSP430x2xx Family User's Guide.*

oscillator and system clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very low power, low frequency oscillator, an internal digitally-controlled oscillator (DCO), and a high frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 μs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal, a high frequency crystal, or the internal very low power LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

DCO Calibration Data (provided from factory in flash info memory segment A)			
DCO Frequency	**Calibration Register**	**Size**	**Address**
1 MHz	CALBC1_1MHZ	byte	010FFh
	CALDCO_1MHZ	byte	010FEh
8 MHz	CALBC1_8MHZ	byte	010FDh
	CALDCO_8MHZ	byte	010FCh
12 MHz	CALBC1_12MHZ	byte	010FBh
	CALDCO_12MHZ	byte	010FAh
16 MHz	CALBC1_16MHZ	byte	010F9h
	CALDCO_16MHZ	byte	010F8h

brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

digital I/O

There are four 8-bit I/O ports implemented—ports P1, P2, P3, and P4:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of port P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup/pulldown resistor.

watchdog timer (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_A3 Signal Connections

Input Pin Number		Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number	
DA	RHA					DA	RHA
31 - P1.0	29 - P1.0	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
9 - P2.1	7 - P2.1	TAINCLK	INCLK				
32 - P1.1	30 - P1.1	TA0	CCI0A	CCR0	TA0	32 - P1.1	30 - P1.1
10 - P2.2	8 - P2.2	TA0	CCI0B			10 - P2.2	8 - P2.2
		V_{SS}	GND			36 - P1.5	34 - P1.5
		V_{CC}	V_{CC}				
33 - P1.2	31 - P1.2	TA1	CCI1A	CCR1	TA1	33 - P1.2	31 - P1.2
29 - P2.3	27 - P2.3	TA1	CCI1B			29 - P2.3	27 - P2.3
		V_{SS}	GND			37 - P1.6	35 - P1.6
		V_{CC}	V_{CC}				
34 - P1.3	32 - P1.3	TA2	CCI2A	CCR2	TA2	34 - P1.3	32 - P1.3
		ACLK (internal)	CCI2B			30 - P2.4	28 - P2.4
		V_{SS}	GND			38 - P1.7	36 - P1.7
		V_{CC}	V_{CC}				

timer_B3

Timer_B3 is a 16-bit timer/counter with three capture/compare registers. Timer_B3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_B3 Signal Connections

Input Pin Number		Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number	
DA	RHA					DA	RHA
24 - P4.7	22 - P4.7	TBCLK	TBCLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
24 - P4.7	22 - P4.7	$\overline{\text{TBCLK}}$	INCLK				
17 - P4.0	15 - P4.0	TB0	CCI0A	CCR0	TB0	17 - P4.0	15 - P4.0
20 - P4.3	18 - P4.3	TB0	CCI0B			20 - P4.3	18 - P4.3
		V_{SS}	GND				
		V_{CC}	V_{CC}				
18 - P4.1	16 - P4.1	TB1	CCI1A	CCR1	TB1	18 - P4.1	16 - P4.1
21 - P4.4	19 - P4.4	TB1	CCI1B			21 - P4.4	19 - P4.4
		V_{SS}	GND				
		V_{CC}	V_{CC}				
19 - P4.2	17 - P4.2	TB2	CCI2A	CCR2	TB2	19 - P4.2	17 - P4.2
		ACLK (internal)	CCI2B			22 - P4.5	20 - P4.5
		V_{SS}	GND				
		V_{CC}	V_{CC}				

universal serial communications interface (USCI)

The USCI module is used for serial data communication. The USCI module supports synchronous communication protocols like SPI (3 or 4 pin), I^2C and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection (LIN), and IrDA.

USCI_A0 provides support for SPI (3 or 4 pin), UART, enhanced UART, and IrDA.

USCI_B0 provides support for SPI (3 or 4 pin) and I^2C.

ADC10

The ADC10 module supports fast, 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator and data transfer controller, or DTC, for automatic conversion result handling allowing ADC samples to be converted and stored without any CPU intervention.

operational amplifier OA (MSP430x22x4 only)

The MSP430x22x4 has two configurable low-current general-purpose operational amplifiers. Each OA input and output terminal is software-selectable and offer a flexible choice of connections for various applications. The OA op amps primarily support front-end analog signal conditioning prior to analog-to-digital conversion.

OA0 Signal Connections

Analog Input Pin Number		Device Input Signal	Module Input Name
DA	RHA		
8 - A0	6 - A0	OA0I0	OAxI0
10 - A2	8 - A2	OA0I1	OA0I1
10 - A2	8 - A2	OA0I1	OAxI1
27 - A6	25 - A6	OA0I2	OAxIA
22 - A14	20 - A14	OA0I3	OAxIB

OA1 Signal Connections

Analog Input Pin Number		Device Input Signal	Module Input Name
DA	RHA		
30 - A4	28 - A4	OA1I0	OAxI0
10 - A2	8 - A2	OA0I1	OA0I1
29 - A3	27 - A3	OA1I1	OAxI1
28 - A7	26 - A7	OA1I2	OAxIA
23 - A15	21 - A15	OA1I3	OAxIB

peripheral file map

PERIPHERALS WITH WORD ACCESS			
ADC10	ADC data transfer start address	ADC10SA	1BCh
	ADC memory	ADC10MEM	1B4h
	ADC control register 1	ADC10CTL1	1B2h
	ADC control register 0	ADC10CTL0	1B0h
	ADC analog enable 0	ADC10AE0	04Ah
	ADC analog enable 1	ADC10AE1	04Bh
	ADC data transfer control register 1	ADC10DTC1	049h
	ADC data transfer control register 0	ADC10DTC0	048h
Timer_B	Capture/compare register	TBCCR2	0196h
	Capture/compare register	TBCCR1	0194h
	Capture/compare register	TBCCR0	0192h
	Timer_B register	TBR	0190h
	Capture/compare control	TBCCTL2	0186h
	Capture/compare control	TBCCTL1	0184h
	Capture/compare control	TBCCTL0	0182h
	Timer_B control	TBCTL	0180h
	Timer_B interrupt vector	TBIV	011Eh
Timer_A	Capture/compare register	TACCR2	0176h
	Capture/compare register	TACCR1	0174h
	Capture/compare register	TACCR0	0172h
	Timer_A register	TAR	0170h
	Capture/compare control	TACCTL2	0166h
	Capture/compare control	TACCTL1	0164h
	Capture/compare control	TACCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Flash Memory	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
Watchdog Timer+	Watchdog/timer control	WDTCTL	0120h
PERIPHERALS WITH BYTE ACCESS			
OA1 (MSP430x22x4 only)	Operational Amplifier 1 control register 1	OA1CTL1	0C3h
	Operational Amplifier 1 control register 1	OA1CTL0	0C2h
OA0 (MSP430x22x4 only)	Operational Amplifier 0 control register 1	OA0CTL1	0C1h
	Operational Amplifier 0 control register 1	OA0CTL0	0C0h
USCI_B0	USCI_B0 transmit buffer	UCB0TXBUF	06Fh
	USCI_B0 receive buffer	UCB0RXBUF	06Eh
	USCI_B0 status	UCB0STAT	06Dh
	USCI_B0 bit rate control 1	UCB0BR1	06Bh
	USCI_B0 bit rate control 0	UCB0BR0	06Ah
	USCI_B0 control 1	UCB0CTL1	069h
	USCI_B0 control 0	UCB0CTL0	068h
	USCI_B0 I2C slave address	UCB0SA	011Ah
	USCI_B0 I2C own address	UCB0OA	0118h
USCI_A0	USCI_A0 transmit buffer	UCA0TXBUF	067h
	USCI_A0 receive buffer	UCA0RXBUF	066h
	USCI_A0 status	UCA0STAT	065h
	USCI_A0 modulation control	UCA0MCTL	064h
	USCI_A0 baud rate control 1	UCA0BR1	063h
	USCI_A0 baud rate control 0	UCA0BR0	062h
	USCI_A0 control 1	UCA0CTL1	061h
	USCI_A0 control 0	UCA0CTL0	060h
	USCI_A0 IrDA receive control	UCA0IRRCTL	05Fh
	USCI_A0 IrDA transmit control	UCA0IRTCTL	05Eh
	USCI_A0 auto baud rate control	UCA0ABCTL	05Dh

PERIPHERALS WITH BYTE ACCESS (continued)			
Basic Clock System+	Basic clock system control 3	BCSCTL3	053h
	Basic clock system control 2	BCSCTL2	058h
	Basic clock system control 1	BCSCTL1	057h
	DCO clock frequency control	DCOCTL	056h
Port P4	Port P4 resistor enable	P4REN	011h
	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 resistor enable	P3REN	010h
	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 resistor enable	P2REN	02Fh
	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 resistor enable	P1REN	027h
	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Function	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

absolute maximum ratings (see Note 1)

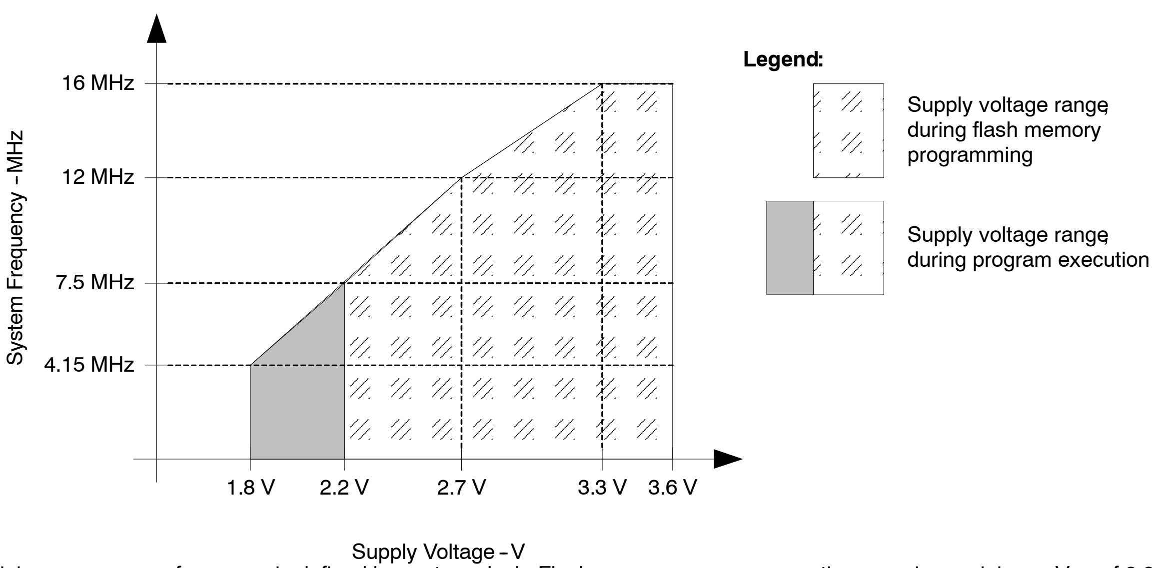
Voltage applied at V_{CC} to V_{SS} .... −0.3 V to 4.1 V
Voltage applied to any pin (see Note 2) .... −0.3 V to V_{CC}+0.3 V
Diode current at any device terminal .... ±2 mA
Storage temperature range, T_{stg}: Unprogrammed device (see Note 3) .... −55°C to 150°C
Programmed device (see Note 3) .... −55°C to 105°C

NOTES: 1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
3. Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage during program execution, V_{CC}		1.8		3.6	V
Supply voltage during program/erase flash memory, V_{CC}		2.2		3.6	V
Supply voltage, V_{SS}			0		V
Operating free-air temperature, T_A	I version	−40		85	°C
	T version	−40		105	°C
Processor frequency, f_{SYSTEM} (maximum MCLK frequency) (see Notes 1 and 2 and Figure 1)	V_{CC} = 1.8 V, Duty cycle = 50% ±10%	dc		4.15	MHz
	V_{CC} = 2.7 V, Duty cycle = 50% ±10%	dc		12	MHz
	V_{CC} ≥ 3.3 V, Duty cycle = 50% ±10%	dc		16	MHz

NOTES: 1. The MSP430 CPU is clocked directly with MCLK.
Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
2. Modules might have a different maximum input clock specification. Refer to the specification of the respective module in this data sheet.



NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 1. Operating Area

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

active mode supply current (into DV_{CC} + AV_{CC}) excluding external current (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{AM,\ 1MHz}$	Active mode (AM) current (1 MHz)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 1 MHz, f_{ACLK} = 32,768 Hz, Program executes in flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		270	390	µA
				3 V		390	550	
$I_{AM,\ 1MHz}$	Active mode (AM) current (1 MHz)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 1 MHz, f_{ACLK} = 32,768 Hz, Program executes in RAM, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		240		µA
				3 V		340		
$I_{AM,\ 4kHz}$	Active mode (AM) current (4 kHz)	f_{MCLK} = f_{SMCLK} = f_{ACLK} = 32,768 Hz/8 = 4,096 Hz, f_{DCO} = 0 Hz, Program executes in flash, SELMx = 11, SELS = 1, DIVMx = DIVSx = DIVAx = 11, CPUOFF = 0, SCG0 = 1, SCG1 = 0, OSCOFF = 0	-40−85°C	2.2 V		5	9	µA
			105°C	2.2 V			18	
			-40−85°C	3 V		6	10	
			105°C	3 V			20	
$I_{AM,100kHz}$	Active mode (AM) current (100 kHz)	f_{MCLK} = f_{SMCLK} = $f_{DCO(0,\ 0)}$ ≈ 100 kHz, f_{ACLK} = 0 Hz, Program executes in flash, RSELx = 0, DCOx = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 1	-40−85°C	2.2 V		60	85	µA
			105°C	2.2 V			95	
			-40−85°C	3 V		72	95	
			105°C	3 V			105	

NOTES: 1. All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
2. The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics - active mode supply current (into DV_{CC} + AV_{CC})

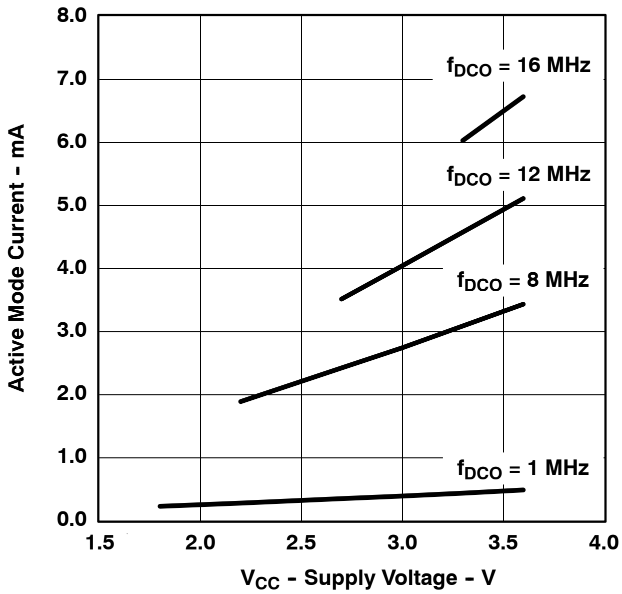


Figure 2. Active Mode Current vs V_{CC}, T_A = 25°C

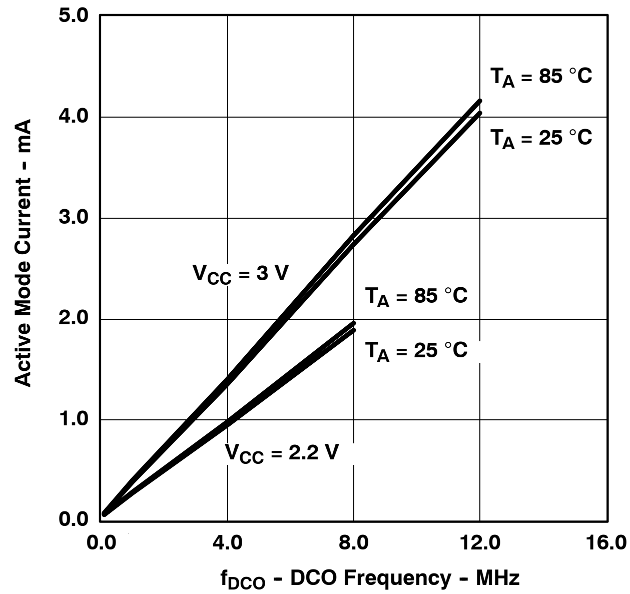


Figure 3. Active Mode Current vs DCO Frequency

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

low power mode supply currents (into DV_{CC} + AV_{CC}) excluding external current (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{LPM0,\ 1MHz}$	Low-power mode 0 (LPM0) current, see Note 3	f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		75	90	μA
				3 V		90	120	
$I_{LPM0,\ 100kHz}$	Low-power mode 0 (LPM0) current, see Note 3	f_{MCLK} = 0 MHz, f_{SMCLK} = $f_{DCO(0,\ 0)}$ ≈ 100 kHz, f_{ACLK} = 0 Hz, RSELx = 0, DCOx = 0, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 1		2.2 V		37	48	μA
				3 V		41	65	
I_{LPM2}	Low-power mode 2 (LPM2) current, see Note 4	f_{MCLK} = f_{SMCLK} = 0 MHz, f_{DCO} = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	-40–85°C	2.2 V		22	29	μA
			105°C				31	
			-40–85°C	3 V		25	32	
			105°C				34	
$I_{LPM3,LFXT1}$	Low-power mode 3 (LPM3) current, see Note 4	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32,768 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-40°C	2.2 V		0.7	1.4	μA
			25°C			0.7	1.4	
			85°C			2.4	3.3	
			105°C			5	10	
			-40°C	3 V		0.9	1.5	
			25°C			0.9	1.5	
			85°C			2.6	3.8	
			105°C			6	12	
$I_{LPM3,VLO}$	Low-power mode 3 current, (LPM3) see Note 4	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-40°C	2.2 V		0.4	1.0	μA
			25°C			0.5	1.0	
			85°C			1.8	2.9	
			105°C			4.5	9	
			-40°C	3 V		0.5	1.2	
			25°C			0.6	1.2	
			85°C			2.1	3.3	
			105°C			5.5	11	
I_{LPM4}	Low-power mode 4 (LPM4) current, see Note 5	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 0 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	-40°C	2.2 V/3 V		0.1	0.5	μA
			25°C			0.1	0.5	
			85°C			1.5	3.0	
			105°C			4.5	9	

NOTES:
1. All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
2. The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.
3. Current for brownout and WDT clocked by SMCLK included.
4. Current for brownout and WDT clocked by ACLK included.
5. Current for brownout included.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

Schmitt-trigger inputs – Ports P1, P2, P3, P4, and $\overline{RST}$/NMI

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			0.45		0.75	V_{CC}
			2.2 V	1.00		1.65	V
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage			0.25		0.55	V_{CC}
			2.2 V	0.55		1.20	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis (V_{IT+} – V_{IT-})		2.2 V	0.2		1.0	V
			3 V	0.3		1.0	
R_{Pull}	Pullup/pulldown resistor	For pullup: $V_{IN} = V_{SS}$; For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

inputs – Ports P1 and P2

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, External trigger pulse width to set interrupt flag (see Note 1)	2.2 V/3 V	20		ns

NOTES: 1. An external signal sets the interrupt flag every time the minimum interrupt puls width $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$.

leakage current – Ports P1, P2, P3 and P4

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.x)}$	High-impedance leakage current	See Notes 1 and 2	2.2 V/3 V		±50	nA

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

outputs – Ports P1, P2, P3 and P4

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = −1.5 mA (see Note 1)	2.2 V	V_{CC}−0.25	V_{CC}	V
		$I_{(OHmax)}$ = −6 mA (see Note 2)	2.2 V	V_{CC}−0.6	V_{CC}	
		$I_{(OHmax)}$ = −1.5 mA (see Note 1)	3 V	V_{CC}−0.25	V_{CC}	
		$I_{(OHmax)}$ = −6 mA (see Note 2)	3 V	V_{CC}−0.6	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1.5 mA (see Note 1)	2.2 V	V_{SS}	V_{SS}+0.25	V
		$I_{(OLmax)}$ = 6 mA (see Note 2)	2.2 V	V_{SS}	V_{SS}+0.6	
		$I_{(OLmax)}$ = 1.5 mA (see Note 1)	3 V	V_{SS}	V_{SS}+0.25	
		$I_{(OLmax)}$ = 6 mA (see Note 2)	3 V	V_{SS}	V_{SS}+0.6	

NOTES: 1. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
2. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

output frequency – Ports P1, P2, P3 and P4

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	P1.4/SMCLK, C_L = 20 pF, R_L = 1 kΩ against $V_{CC}/2$ (see Notes 1 and 2)	2.2 V		10	MHz
			3 V		12	
f_{Port_CLK}	Clock output frequency	P2.0/ACLK, P1.4/SMCLK, C_L = 20 pF (see Note 2)	2.2 V		12	MHz
			3 V		16	

NOTES: 1. Alternatively a resistive divider with 2 times 2 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
2. The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics − outputs

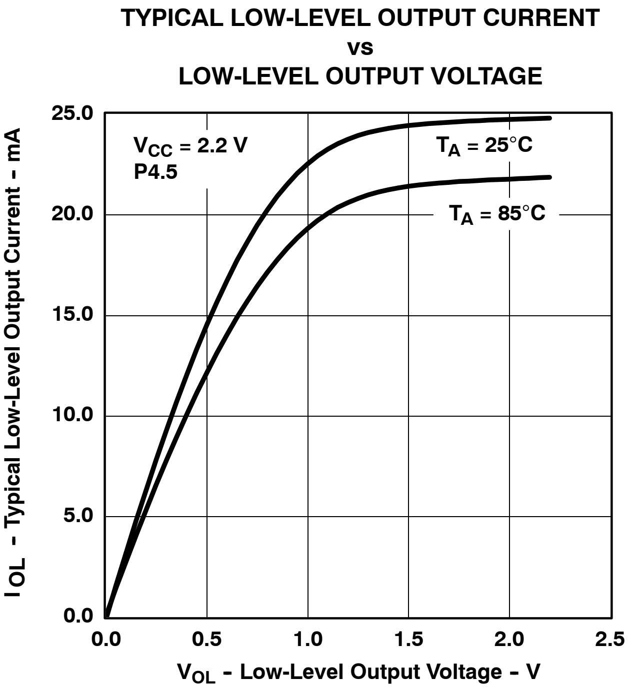


Figure 4

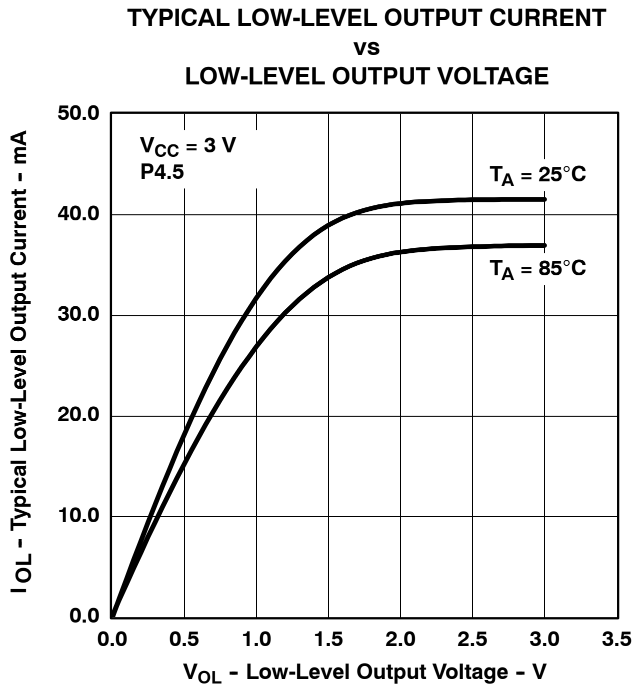


Figure 5

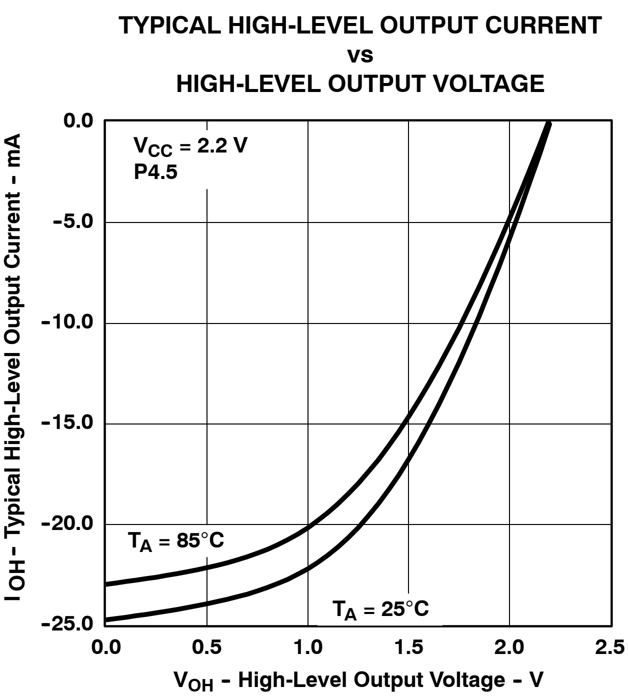


Figure 6

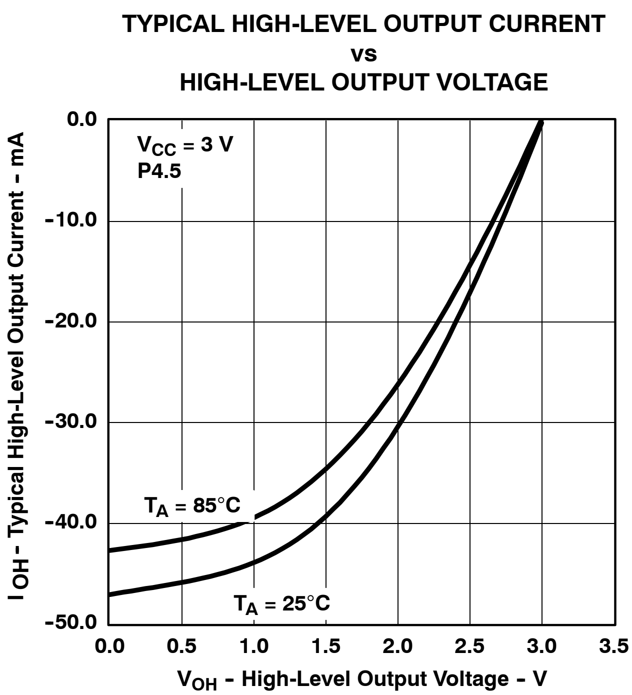


Figure 7

NOTE: One output loaded at a time

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

POR/brownout reset (BOR) (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(start)}$	See Figure 8	$dV_{CC}/dt \le 3$ V/s			$0.7 \times V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$	See Figure 8 through Figure 10	$dV_{CC}/dt \le 3$ V/s				1.71	V
$V_{hys(B\_IT-)}$	See Figure 8	$dV_{CC}/dt \le 3$ V/s		70	130	210	mV
$t_{d(BOR)}$	See Figure 8					2000	μs
$t_{(reset)}$	Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally		2.2 V/3 V	2			μs

NOTES: 1. The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8V.
2. During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default DCO settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency.

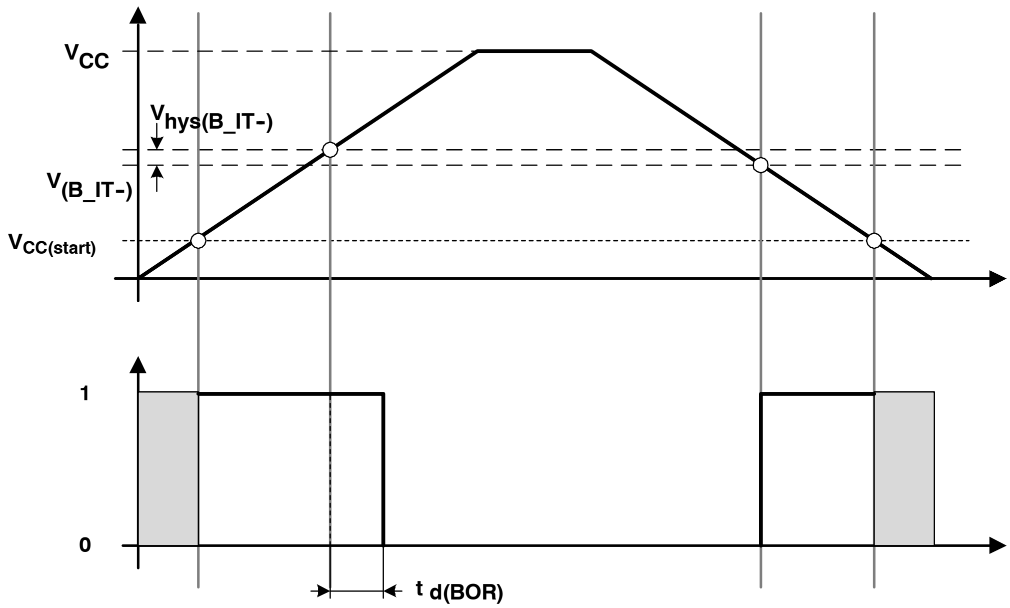


Figure 8. POR/Brownout Reset (BOR) vs Supply Voltage

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics − POR/brownout reset (BOR)

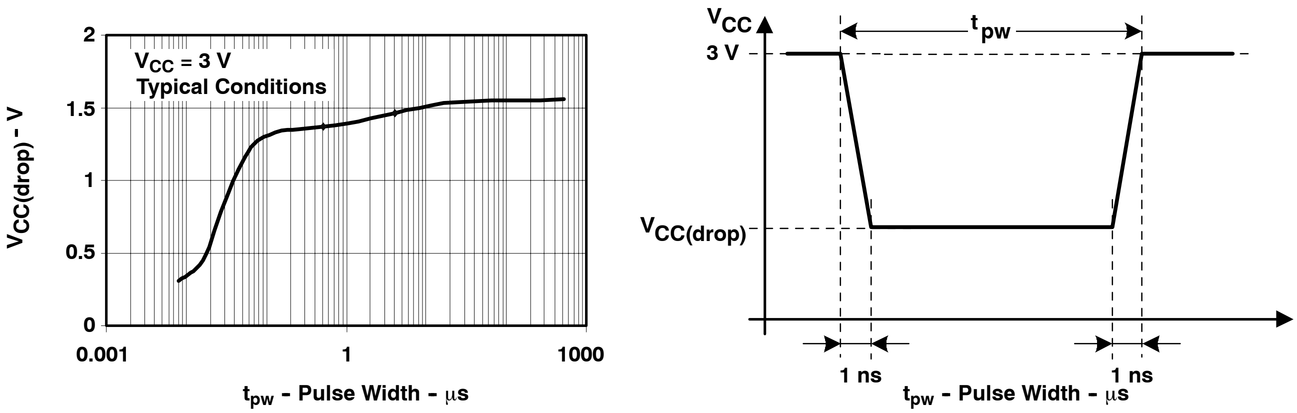


Figure 9. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

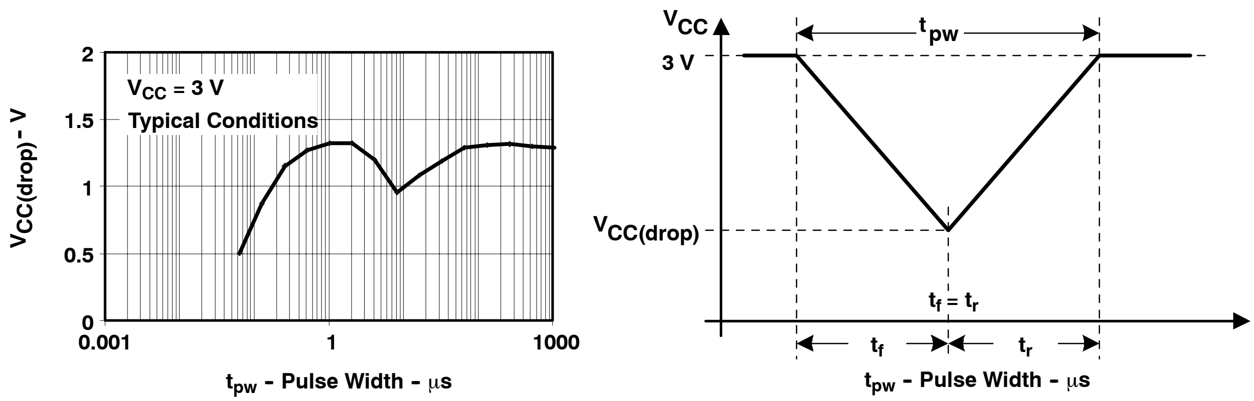


Figure 10. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

main DCO characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO}.
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

DCO frequency

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Vcc	Supply voltage range	RSELx < 14		1.8		3.6	V
		RSELx = 14		2.2		3.6	
		RSELx = 15		3.0		3.6	
$f_{DCO(0,0)}$	DCO frequency (0, 0)	RSELx = 0, DCOx = 0, MODx = 0	2.2 V/3 V	0.06		0.14	MHz
$f_{DCO(0,3)}$	DCO frequency (0, 3)	RSELx = 0, DCOx = 3, MODx = 0	2.2 V/3 V	0.07		0.17	MHz
$f_{DCO(1,3)}$	DCO frequency (1, 3)	RSELx = 1, DCOx = 3, MODx = 0	2.2 V/3 V	0.10		0.20	MHz
$f_{DCO(2,3)}$	DCO frequency (2, 3)	RSELx = 2, DCOx = 3, MODx = 0	2.2 V/3 V	0.14		0.28	MHz
$f_{DCO(3,3)}$	DCO frequency (3, 3)	RSELx = 3, DCOx = 3, MODx = 0	2.2 V/3 V	0.20		0.40	MHz
$f_{DCO(4,3)}$	DCO frequency (4, 3)	RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V	0.28		0.54	MHz
$f_{DCO(5,3)}$	DCO frequency (5, 3)	RSELx = 5, DCOx = 3, MODx = 0	2.2 V/3 V	0.39		0.77	MHz
$f_{DCO(6,3)}$	DCO frequency (6, 3)	RSELx = 6, DCOx = 3, MODx = 0	2.2 V/3 V	0.54		1.06	MHz
$f_{DCO(7,3)}$	DCO frequency (7, 3)	RSELx = 7, DCOx = 3, MODx = 0	2.2 V/3 V	0.80		1.50	MHz
$f_{DCO(8,3)}$	DCO frequency (8, 3)	RSELx = 8, DCOx = 3, MODx = 0	2.2 V/3 V	1.10		2.10	MHz
$f_{DCO(9,3)}$	DCO frequency (9, 3)	RSELx = 9, DCOx = 3, MODx = 0	2.2 V/3 V	1.60		3.00	MHz
$f_{DCO(10,3)}$	DCO frequency (10, 3)	RSELx = 10, DCOx = 3, MODx = 0	2.2 V/3 V	2.50		4.30	MHz
$f_{DCO(11,3)}$	DCO frequency (11, 3)	RSELx = 11, DCOx = 3, MODx = 0	2.2 V/3 V	3.00		5.50	MHz
$f_{DCO(12,3)}$	DCO frequency (12, 3)	RSELx = 12, DCOx = 3, MODx = 0	2.2 V/3 V	4.30		7.30	MHz
$f_{DCO(13,3)}$	DCO frequency (13, 3)	RSELx = 13, DCOx = 3, MODx = 0	2.2 V/3 V	6.00		9.60	MHz
$f_{DCO(14,3)}$	DCO frequency (14, 3)	RSELx = 14, DCOx = 3, MODx = 0	2.2 V/3 V	8.60		13.9	MHz
$f_{DCO(15,3)}$	DCO frequency (15, 3)	RSELx = 15, DCOx = 3, MODx = 0	3 V	12.0		18.5	MHz
$f_{DCO(15,7)}$	DCO frequency (15, 7)	RSELx = 15, DCOx = 7, MODx = 0	3 V	16.0		26.0	MHz
S_{RSEL}	Frequency step between range RSEL and RSEL+1	$S_{RSEL} = f_{DCO(RSEL+1,DCO)}/f_{DCO(RSEL,DCO)}$	2.2 V/3 V			1.55	ratio
S_{DCO}	Frequency step between tap DCO and DCO+1	$S_{DCO} = f_{DCO(RSEL,DCO+1)}/f_{DCO(RSEL,DCO)}$	2.2 V/3 V	1.05	1.08	1.12	ratio
Duty Cycle		Measured at P1.4/SMCLK	2.2 V/3 V	40	50	60	%

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

calibrated DCO frequencies − tolerance at calibration

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
Frequency tolerance at calibration			25°C	3 V	−1	±0.2	+1	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1= CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	25°C	3 V	0.990	1	1.010	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1= CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	25°C	3 V	7.920	8	8.080	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1= CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	25°C	3 V	11.88	12	12.12	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1= CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	25°C	3 V	15.84	16	16.16	MHz

calibrated DCO frequencies − tolerance over temperature 0°C to +85°C

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance over temperature			0−85°C	3.0 V	−2.5	±0.5	+2.5	%
8-MHz tolerance over temperature			0−85°C	3.0 V	−2.5	±1.0	+2.5	%
12-MHz tolerance over temperature			0−85°C	3.0 V	−2.5	±1.0	+2.5	%
16-MHz tolerance over temperature			0−85°C	3.0 V	−3.0	±2.0	+3.0	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1= CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	0−85°C	2.2 V	0.970	1	1.030	MHz
				3.0 V	0.975	1	1.025	
				3.6 V	0.970	1	1.030	
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1= CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	0−85°C	2.2 V	7.760	8	8.400	MHz
				3.0 V	7.800	8	8.200	
				3.6 V	7.600	8	8.240	
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1= CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	0−85°C	2.2 V	11.70	12	12.30	MHz
				3.0 V	11.70	12	12.30	
				3.6 V	11.70	12	12.30	
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1= CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	0−85°C	3.0 V	15.52	16	16.48	MHz
				3.6 V	15.00	16	16.48	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

calibrated DCO frequencies - tolerance over supply voltage V_{CC}

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance over V_{CC}			25°C	1.8 V − 3.6 V	−3	±2	+3	%
8-MHz tolerance over V_{CC}			25°C	1.8 V − 3.6 V	−3	±2	+3	%
12-MHz tolerance over V_{CC}			25°C	2.2 V − 3.6 V	−3	±2	+3	%
16 -Hz tolerance over V_{CC}			25°C	3.0 V − 3.6 V	−6	±2	+3	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1= CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	25°C	1.8 V − 3.6 V	0.970	1	1.030	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1= CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	25°C	1.8 V − 3.6 V	7.760	8	8.240	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1= CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	25°C	2.2 V − 3.6 V	11.64	12	12.36	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1= CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	25°C	3.0 V − 3.6 V	15.00	16	16.48	MHz

calibrated DCO frequencies - overall tolerance

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance overall			I: -40−85°C T: -40−105°C	1.8 V to 3.6 V	−5	±2	+5	%
8-MHz tolerance overall			I: -40−85°C T: -40−105°C	1.8 V to 3.6 V	−5	±2	+5	%
12-MHz tolerance overall			I: -40−85°C T: -40−105°C	2.2 V to 3.6 V	−5	±2	+5	%
16-MHz tolerance overall			I: -40−85°C T: -40−105°C	3.0 V to 3.6 V	−6	±3	+6	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1= CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	I: -40−85°C T: -40−105°C	1.8 V to 3.6 V	0.950	1	1.050	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1= CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	I: -40−85°C T: -40−105°C	1.8 V to 3.6 V	7.600	8	8.400	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1= CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	I: -40−85°C T: -40−105°C	2.2 V to 3.6 V	11.40	12	12.60	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1= CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	I: -40−85°C T: -40−105°C	3.0 V to 3.6 V	15.00	16	17.00	MHz

typical characteristics − calibrated 1-MHz DCO frequency

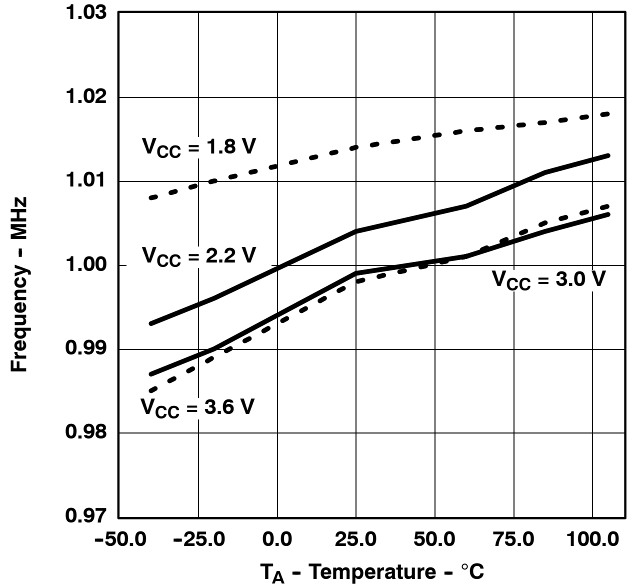


Figure 11. Calibrated 1-MHz Frequency vs Temperature

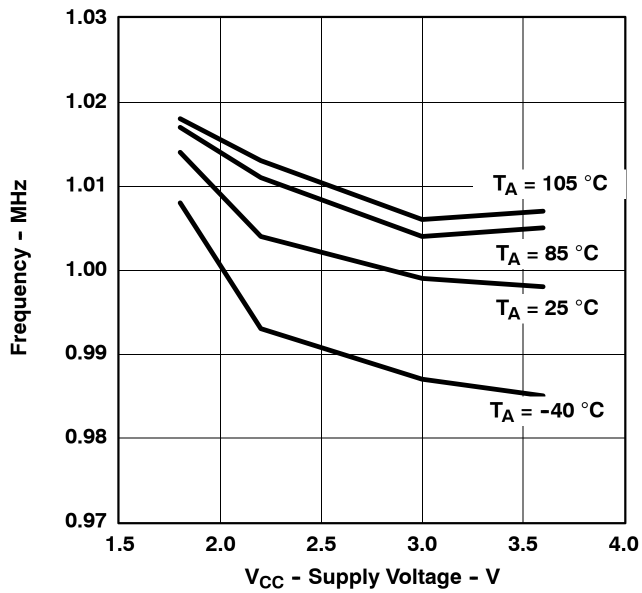


Figure 12. Calibrated 1-MHz Frequency vs V_{CC}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

wake-up from lower power modes (LPM3/4)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{DCO,LPM3/4}$	DCO clock wake-up time from LPM3/4 (see Note 1)	BCSCTL1= CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ	2.2 V/3 V			2	μs
		BCSCTL1= CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ	2.2 V/3 V			1.5	
		BCSCTL1= CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ	2.2 V/3 V			1	
		BCSCTL1= CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ	3 V			1	
$t_{CPU,LPM3/4}$	CPU wake-up time from LPM3/4 (see Note 2)					$1/f_{MCLK} + t_{Clock,LPM3/4}$	

NOTES: 1. The DCO clock wake-up time is measured from the edge of an external wake-up signal (e.g., port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
2. Parameter applicable only if DCOCLK is used for MCLK.

typical characteristics – DCO clock wake-up time from LPM3/4

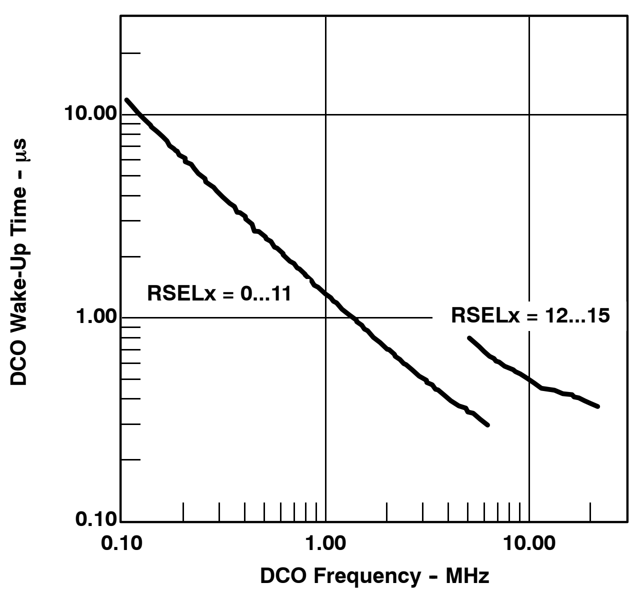


Figure 13. Clock Wake-Up Time From LPM3 vs DCO Frequency

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

DCO with external resistor R_{OSC} (see Note 1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{DCO,ROSC}$	DCO output frequency with R_{OSC}	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0, T_A = 25°C	2.2 V		1.8		MHz
			3 V		1.95		
D_t	Temperature drift	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V		±0.1		%/°C
D_V	Drift with V_{CC}	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V		10		%/V

NOTES: 1. R_{OSC} = 100kΩ. Metal film resistor, type 0257. 0.6 watt with 1% tolerance and T_K = ±50ppm/°C.

typical characteristics − DCO with external resistor R_{OSC}

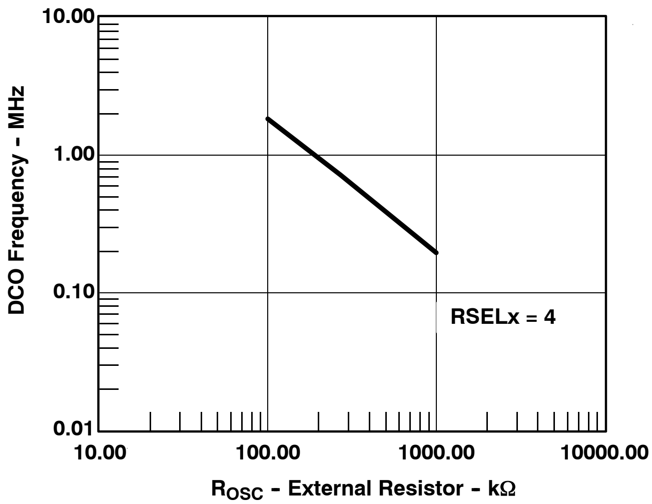


Figure 14. DCO Frequency vs R_{OSC}, V_{CC} = 2.2 V, T_A = 25°C

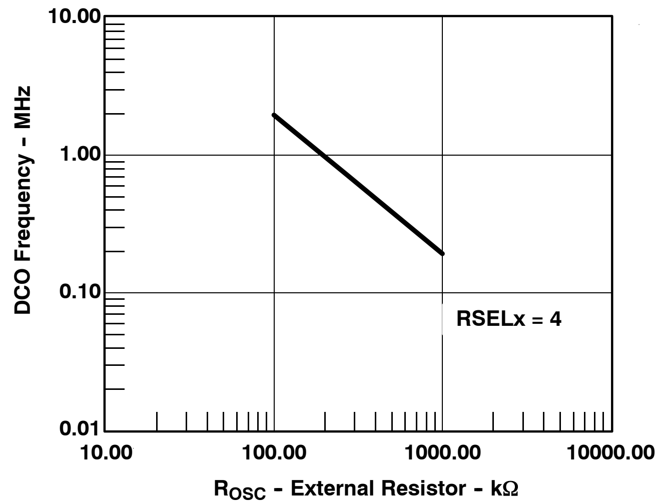


Figure 15. DCO Frequency vs R_{OSC}, V_{CC} = 3.0 V, T_A = 25°C

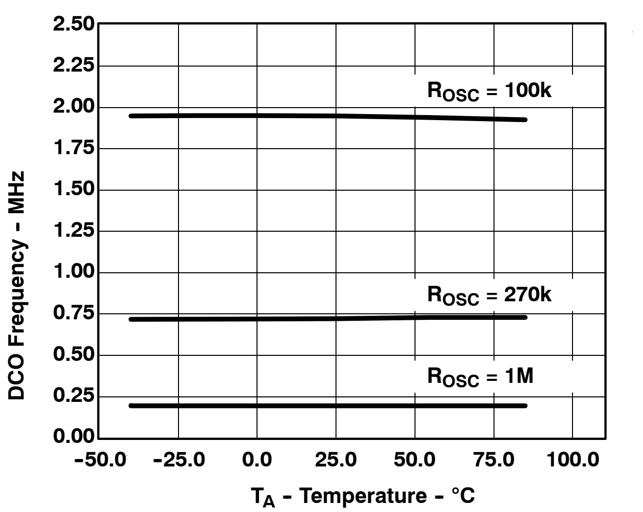


Figure 16. DCO Frequency vs Temperature, V_{CC} = 3.0 V

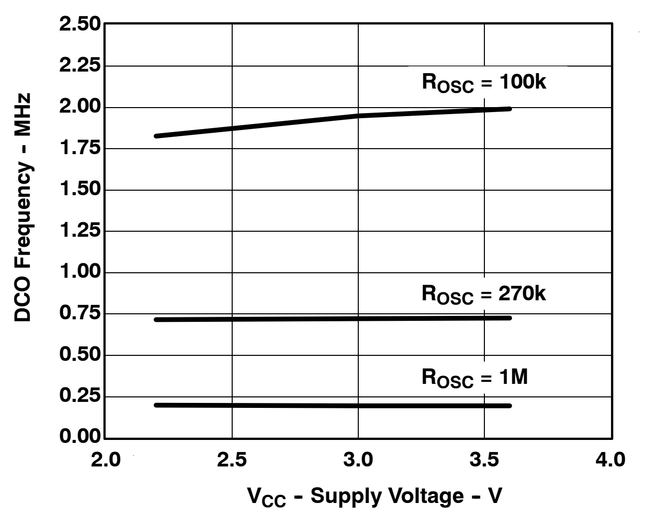


Figure 17. DCO Frequency vs V_{CC}, T_A = 25°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator, LFXT1, low frequency modes (see Note 4)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,LF}$	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1	1.8 V to 3.6 V		32,768		Hz
$f_{LFXT1,LF,logic}$	LFXT1 oscillator logic level square wave input frequency, LF mode	XTS = 0, LFXT1Sx = 3	1.8 V to 3.6 V	10,000	32,768	50,000	Hz
OA_{LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0; $f_{LFXT1,LF}$ = 32,768 kHz, $C_{L,eff}$ = 6 pF			500		kΩ
		XTS = 0, LFXT1Sx = 0; $f_{LFXT1,LF}$ = 32,768 kHz, $C_{L,eff}$ = 12 pF			200		
$C_{L,eff}$	Integrated effective load capacitance, LF mode (see Note 1)	XTS = 0, XCAPx = 0			1		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			11		
Duty Cycle	LF mode	XTS = 0, Measured at P1.4/ACLK, $f_{LFXT1,LF}$ = 32,768 Hz	2.2 V/3 V	30	50	70	%
$f_{Fault,LF}$	Oscillator fault frequency, LF mode (see Note 3)	XTS = 0, LFXT1Sx = 3 (see Note 2)	2.2 V/3 V	10		10,000	Hz

NOTES: 1. Includes parasitic bond and package capacitance (approximately 2pF per pin).
Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Measured with logic level input frequency but also applies to operation with crystals.
3. Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
4. To improve EMI on the LFXT1 oscillator the following guidelines should be observed.
- Keep as short a trace as possible between the device and the crystal.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
- Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

internal very low power, low frequency oscillator (VLO)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency		-40−85°C	2.2 V/3 V	4	12	20	kHz
			105°C	2.2 V/3 V			22	
df_{VLO}/dT	VLO frequency temperature drift	(see Note 1)	I: -40−85°C T: -40−105°C	2.2 V/3 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	(see Note 2)	25°C	1.8V to 3.6V		4		%/V

NOTES: 1. Calculated using the box method:
I version: (MAX(−40...85°C) − MIN(−40...85°C))/MIN(−40...85°C)/(85°C − (−40°C))
T version: (MAX(−40...105°C) − MIN(−40...105°C))/MIN(−40...105°C)/(105°C − (−40°C))
2. Calculated using the box method: (MAX(1.8...3.6 V) − MIN(1.8...3.6 V))/MIN(1.8...3.6V)/(3.6 V − 1.8 V)

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator, LFXT1, high frequency modes (see Note 5)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,HF0}$	LFXT1 oscillator crystal frequency, HF mode 0	XTS = 1, LFXT1Sx = 0	1.8 V to 3.6 V	0.4		1	MHz
$f_{LFXT1,HF1}$	LFXT1 oscillator crystal frequency, HF mode 1	XTS = 1, LFXT1Sx = 1	1.8 V to 3.6 V	1		4	MHz
$f_{LFXT1,HF2}$	LFXT1 oscillator crystal frequency, HF mode 2	XTS = 1, LFXT1Sx = 2	1.8 V to 3.6 V	2		10	MHz
			2.2 V to 3.6 V	2		12	
			3.0 V to 3.6 V	2		16	
$f_{LFXT1,HF,logic}$	LFXT1 oscillator logic level square-wave input frequency, HF mode	XTS = 1, LFXT1Sx = 3	1.8 V to 3.6 V	0.4		10	MHz
			2.2 V to 3.6 V	0.4		12	
			3.0 V to 3.6 V	0.4		16	
OA_{HF}	Oscillation allowance for HF crystals (see Figure 18 and Figure 19)	XTS = 0, LFXT1Sx = 0, $f_{LFXT1,HF}$ = 1 MHz, $C_{L,eff}$ = 15 pF			2700		Ω
		XTS = 0, LFXT1Sx = 1 $f_{LFXT1,HF}$ = 4 MHz, $C_{L,eff}$ = 15 pF			800		
		XTS = 0, LFXT1Sx = 2 $f_{LFXT1,HF}$ = 16 MHz, $C_{L,eff}$ = 15 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, HF mode (see Note 1)	XTS = 1 (see Note 2)			1		pF
Duty Cycle	HF mode	XTS = 1, Measured at P1.4/ACLK, $f_{LFXT1,HF}$ = 10 MHz	2.2 V/3 V	40	50	60	%
		XTS = 1, Measured at P1.4/ACLK, $f_{LFXT1,HF}$ = 16 MHz	2.2 V/3 V	40	50	60	
$f_{Fault,HF}$	Oscillator fault frequency, HF mode (see Note 4)	XTS = 1, LFXT1Sx = 3 (see Notes 3)	2.2 V/3 V	30		300	kHz

NOTES: 1. Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
3. Measured with logic level input frequency but also applies to operation with crystals.
4. Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
5. To improve EMI on the LFXT1 oscillator the following guidelines should be observed.
   - Keep the trace between the device and the crystal as short as possible.
   - Design a good ground plane around the oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics − LFXT1 oscillator in HF mode (XTS = 1)

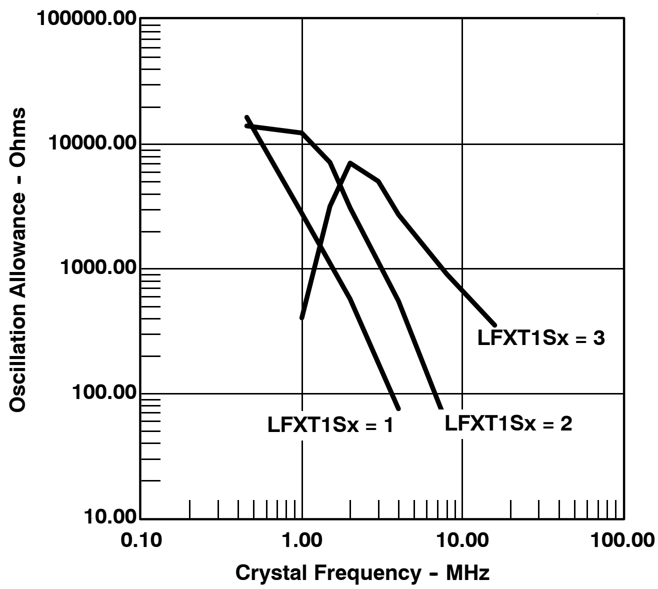


Figure 18. Oscillation Allowance vs Crystal Frequency, $C_{L,eff}$ = 15 pF, T_A = 25°C

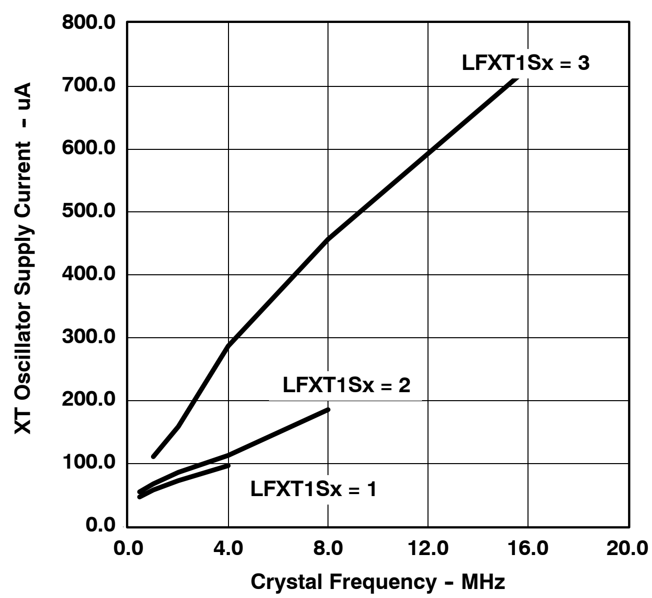


Figure 19. XT Oscillator Supply Current vs Crystal Frequency, $C_{L,eff}$ = 15 pF, T_A = 25°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

Timer_A

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{TA}	Timer_A clock frequency	Internal: SMCLK, ACLK, External: TACLK, INCLK, Duty cycle = 50% ±10%	2.2 V		10	MHz
			3 V		16	
$t_{TA,cap}$	Timer_A, capture timing	TA0, TA1, TA2	2.2 V/3 V	20		ns

Timer_B

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{TB}	Timer_B clock frequency	Internal: SMCLK, ACLK, External: TBCLK, Duty cycle = 50% ±10%	2.2 V		10	MHz
			3 V		16	
$t_{TB,cap}$	Timer_B, capture timing	TB0, TB1, TB2	2.2 V/3 V	20		ns

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

USCI (UART mode)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)		2.2V /3 V			1	MHz
t_{τ}	UART receive deglitch time (see Note 1)		2.2 V	50	150	600	ns
			3 V	50	100	600	ns

NOTES: 1. Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their width should exceed the maximum specification of the deglitch time.

USCI (SPI master mode) (see Figure 20 and Figure 21)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, ACLK Duty cycle = 50% ± 10%			f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time		2.2 V	110		ns
			3 V	75		ns
$t_{HD,MI}$	SOMI input data hold time		2.2 V	0		ns
			3 V	0		ns
$t_{VALID,MO}$	SIMO output data valid time	UCLK edge to SIMO valid, C_L = 20 pF	2.2 V		30	ns
			3 V		20	ns

NOTE: $f_{UCxCLK} = \frac{1}{2t_{LO/HI}}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$.
For the slave's parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.

USCI (SPI slave mode) (see Figure 22 and Figure 23)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time STE low to clock		2.2 V/3 V		50		ns
$t_{STE,LAG}$	STE lag time Last clock to STE high		2.2 V/3 V	10			ns
$t_{STE,ACC}$	STE access time STE low to SOMI data out		2.2 V/3 V		50		ns
$t_{STE,DIS}$	STE disable time STE high to SOMI high impedance		2.2 V/3 V		50		ns
$t_{SU,SI}$	SIMO input data setup time		2.2 V	20			ns
			3 V	15			ns
$t_{HD,SI}$	SIMO input data hold time		2.2 V	10			ns
			3 V	10			ns
$t_{VALID,SO}$	SOMI output data valid time	UCLK edge to SOMI valid, C_L = 20 pF	2.2 V		75	110	ns
			3 V		50	75	ns

NOTE: $f_{UCxCLK} = \frac{1}{2t_{LO/HI}}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$.
For the master's parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

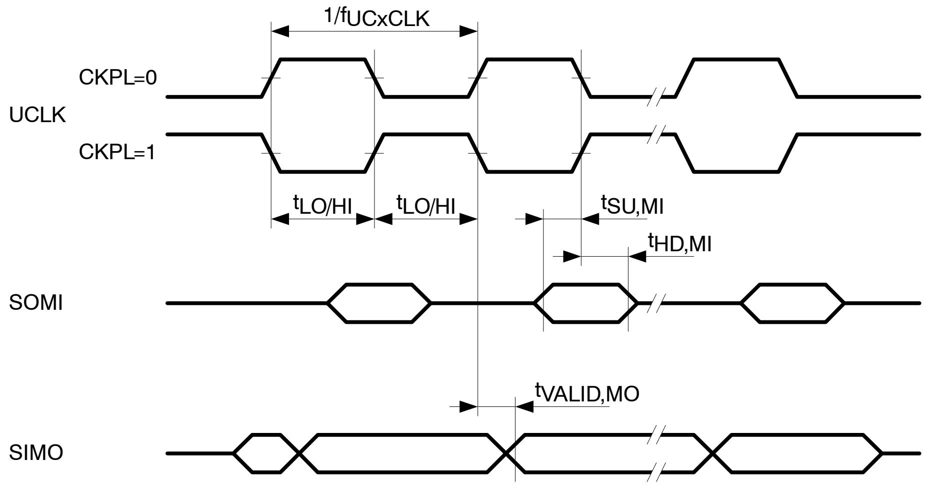


Figure 20. SPI Master Mode, CKPH = 0

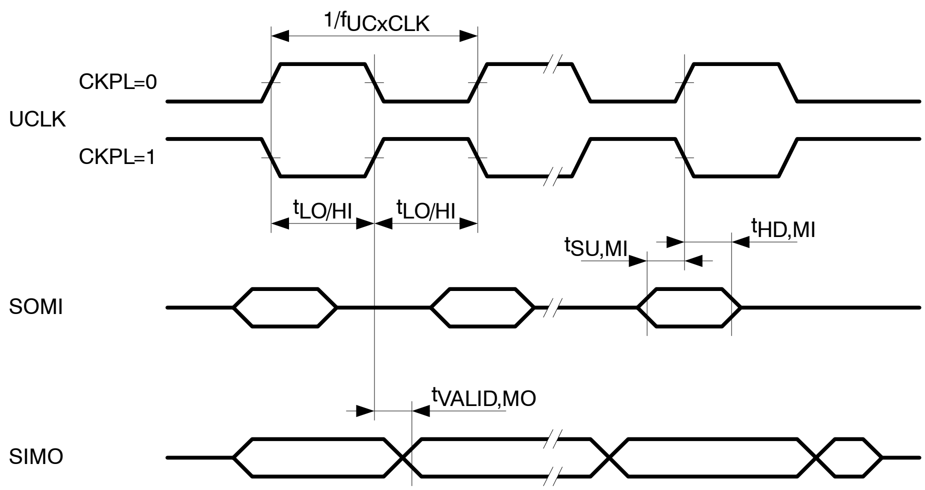


Figure 21. SPI Master Mode, CKPH = 1

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

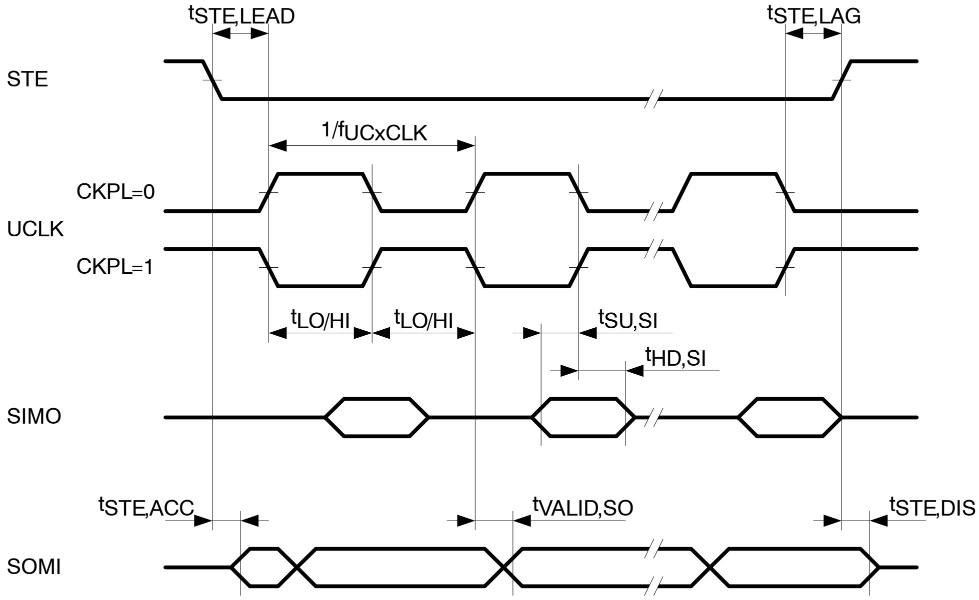


Figure 22. SPI Slave Mode, CKPH = 0

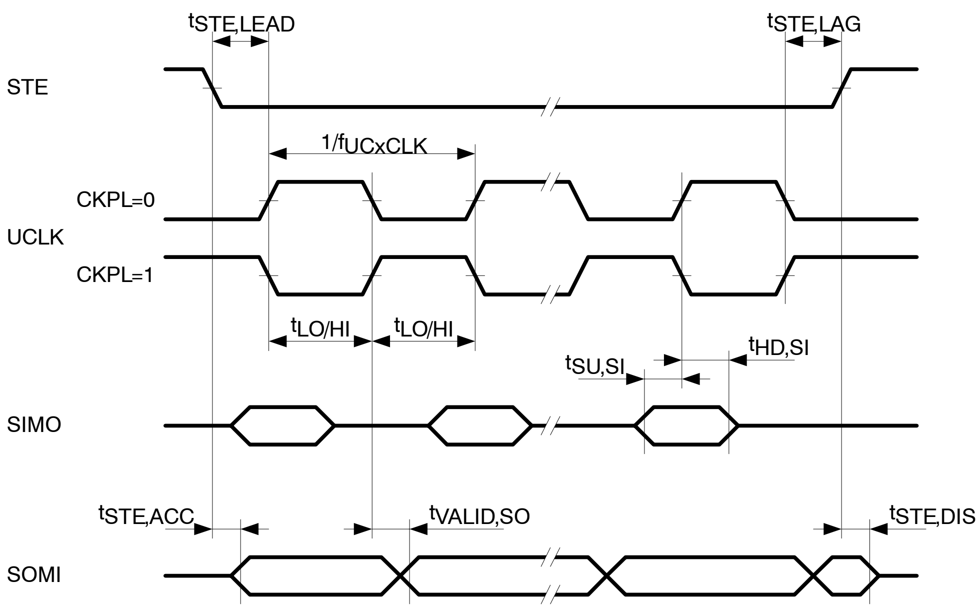


Figure 23. SPI Slave Mode, CKPH = 1

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

USCI (I2C mode) (see Figure 24)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V/3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	2.2 V/3 V	4.0			µs
		f_{SCL} > 100 kHz	2.2 V/3 V	0.6			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	2.2 V/3 V	4.7			µs
		f_{SCL} > 100 kHz	2.2 V/3 V	0.6			
$t_{HD,DAT}$	Data hold time		2.2 V/3 V	0			ns
$t_{SU,DAT}$	Data setup time		2.2 V/3 V	250			ns
$t_{SU,STO}$	Setup time for STOP		2.2 V/3 V	4.0			µs
t_{SP}	Pulse width of spikes suppressed by input filter		2.2 V	50	150	600	ns
			3 V	50	100	600	

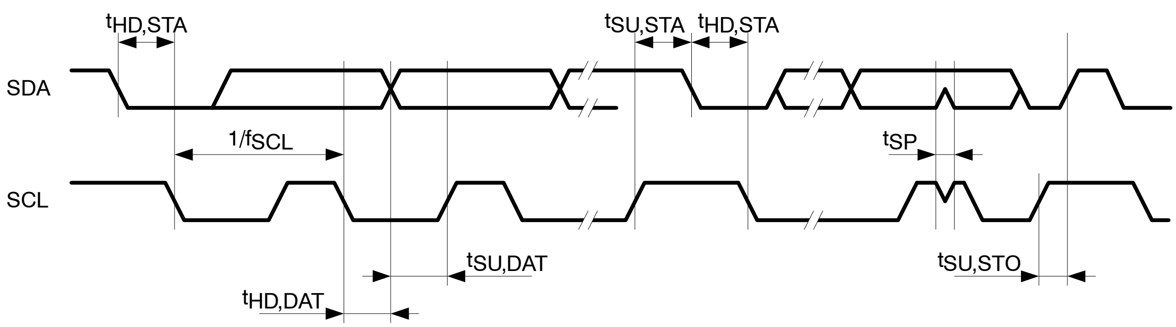


Figure 24. I2C Mode Timing

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

10-bit ADC, power supply and input range conditions (see Note 1)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Analog supply voltage range	V_{SS} = 0 V			2.2		3.6	V
V_{Ax}	Analog input voltage range (see Note 2)	All Ax terminals. Analog inputs selected in ADC10AE register			0		V_{CC}	V
I_{ADC10}	ADC10 supply current (see Note 3)	$f_{ADC10CLK}$ = 5.0 MHz ADC10ON = 1, REFON = 0, ADC10SHT0 = 1, ADC10SHT1 = 0, ADC10DIV = 0	I: -40−85°C T: -40−105°C	2.2 V		0.52	1.05	mA
				3 V		0.6	1.2	
I_{REF+}	Reference supply current, reference buffer disabled (see Note 4)	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REF2_5V = 0, REFON = 1, REFOUT = 0	I: -40−85°C T: -40−105°C	2.2 V/3 V		0.25	0.4	mA
		$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REF2_5V = 1, REFON = 1, REFOUT = 0	I: -40−85°C T: -40−105°C	3 V				
$I_{REFB,0}$	Reference buffer supply current with ADC10SR = 0 (see Note 4)	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR=0	-40−85°C	2.2 V/3 V		1.1	1.4	mA
			105°C	2.2 V/3 V			1.8	
$I_{REFB,1}$	Reference buffer supply current with ADC10SR = 1 (see Note 4)	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR=1	-40−85°C	2.2 V/3 V		0.5	0.7	mA
			105°C	2.2 V/3 V			0.8	
C_I	Input capacitance	Only one terminal Ax selected at a time	I: -40−85°C T: -40−105°C				27	pF
R_I	Input MUX ON resistance	0V ≤ V_{Ax} ≤ V_{CC}	I: -40−85°C T: -40−105°C	2.2 V/3 V			2000	Ω

NOTES:
1. The leakage current is defined in the leakage current table with Px.x/Ax parameter.
2. The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
3. The internal reference supply current is not included in current consumption parameter I_{ADC10}.
4. The internal reference current is supplied via terminal V_{CC}. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

10-bit ADC, built-in voltage reference

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC,REF+}$	Positive built-in reference analog supply voltage range	I_{VREF+} ≤ 1 mA, REF2_5V = 0			2.2			V
		I_{VREF+} ≤ 0.5 mA, REF2_5V = 1			2.8			
		I_{VREF+} ≤ 1 mA, REF2_5V = 1			2.9			
V_{REF+}	Positive built-in reference voltage	I_{VREF+} ≤ I_{VREF+}max, REF2_5V = 0		2.2 V/3 V	1.41	1.5	1.59	V
		I_{VREF+} ≤ I_{VREF+}max, REF2_5V = 1		3 V	2.35	2.5	2.65	
$I_{LD,VREF+}$	Maximum V_{REF+} load current			2.2 V			±0.5	mA
				3 V			±1	
	V_{REF+} load regulation	I_{VREF+} = 500 µA ± 100 µA, Analog input voltage V_{Ax} ≈ 0.75 V, REF2_5V = 0		2.2 V/3 V			±2	LSB
		I_{VREF+} = 500 µA ± 100 µA, Analog input voltage V_{Ax} ≈ 1.25 V, REF2_5V = 1		3 V			±2	
	V_{REF+} load regulation response time	I_{VREF+} = 100 µA → 900 µA, V_{Ax} ≈ 0.5 x V_{REF+}, Error of conversion result ≤1 LSB	ADC10SR=0	3 V			400	ns
			ADC10SR=1				2000	
C_{VREF+}	Max. capacitance at pin V_{REF+} (see Note 1)	I_{VREF+} ≤ ±1 mA, REFON = 1, REFOUT = 1		2.2 V/3 V			100	pF
TC_{REF+}	Temperature coefficient	I_{VREF+} = const. with 0 mA ≤ I_{VREF+} ≤ 1 mA		2.2 V/3 V			±100	ppm/°C
t_{REFON}	Settling time of internal reference voltage (see Note 2)	I_{VREF+} = 0.5 mA, REF2_5V = 0, REFON = 0 → 1		3.6 V			30	µs
$t_{REFBURST}$	Settling time of reference buffer (see Note 2)	I_{VREF+} = 0.5 mA, REF2_5V = 0, REFON = 1, REFBURST = 1	ADC10SR=0	2.2 V			1	µs
			ADC10SR=1				2.5	
		I_{VREF+} = 0.5 mA, REF2_5V = 1, REFON = 1, REFBURST = 1	ADC10SR=0	3 V			2	
			ADC10SR=1				4.5	

NOTES:
1. The capacitance applied to the internal buffer operational amplifier, if switched to terminal P2.4/TA2/A4/V_{REF+}/V_{eREF+} (REFOUT=1), must be limited; the reference buffer may become unstable otherwise.
2. The condition is that the error in a conversion started after t_{REFON} or t_{RefBuf} is less than ±0.5 LSB.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

10-bit ADC, external reference (see Note 1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{eREF+}	Positive external reference input voltage range (see Note 2)	$V_{eREF+} > V_{eREF-}$, SREF1 = 1, SREF0 = 0		1.4	V_{CC}	V
		$V_{eREF-} \leq V_{eREF+} \leq V_{CC} - 0.15$ V, SREF1 = 1, SREF0 = 1 (see Note 3)		1.4	3.0	
V_{eREF-}	Negative external reference input voltage range (see Note 4)	$V_{eREF+} > V_{eREF-}$		0	1.2	V
ΔV_{eREF}	Differential external reference input voltage range $\Delta V_{eREF} = V_{eREF+} - V_{eREF-}$	$V_{eREF+} > V_{eREF-}$ (see Note 5)		1.4	V_{CC}	V
I_{VeREF+}	Static input current into V_{eREF+}	$0V \leq V_{eREF+} \leq V_{CC}$, SREF1 = 1, SREF0 = 0	2.2 V/3 V		±1	µA
		$0V \leq V_{eREF+} \leq V_{CC} - 0.15\ V \leq 3$ V, SREF1 = 1, SREF0 = 1 (see Note 3)			0	
I_{VeREF-}	Static input current into V_{eREF-}	$0V \leq V_{eREF-} \leq V_{CC}$	2.2 V/3 V		±1	µA

NOTES: 1. The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
2. The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
3. Under this condition, the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current I_{REFB}. The current consumption can be limited to the sample and conversion period with REBURST = 1.
4. The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
5. The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

10-bit ADC, timing parameters

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC10CLK}$	ADC10 input clock frequency	For specified performance of ADC10 linearity parameters	ADC10SR=0	2.2 V/3 V	0.45		6.3	MHz
			ADC10SR=1		0.45		1.5	
$f_{ADC10OSC}$	ADC10 built-in oscillator frequency	ADC10DIVx = 0, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$		2.2 V/3 V	3.7		6.3	MHz
$t_{CONVERT}$	Conversion time	ADC10 built-in oscillator, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$		2.2 V/3 V	2.06		3.51	μs
		$f_{ADC10CLK}$ from ACLK, MCLK or SMCLK, ADC10SSELx ≠ 0				13× ADC10DIV× $1/f_{ADC10CLK}$		
$t_{ADC10ON}$	Turn on settling time of the ADC	(see Note 1)					100	ns

NOTES: 1. The condition is that the error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.

10-bit ADC, linearity parameters

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error		2.2 V/3 V			±1	LSB
E_D	Differential linearity error		2.2 V/3 V			±1	LSB
E_O	Offset error	Source impedance R_S < 100 Ω,	2.2 V/3 V			±1	LSB
E_G	Gain error	SREFx = 010, unbuffered external reference, V_{eREF+} = 1.5 V	2.2 V		±1.1	±2	LSB
		SREFx = 010, unbuffered external reference, V_{eREF+} = 2.5 V	3 V		±1.1	±2	
		SREFx = 011, buffered external reference (see Note 1), V_{eREF+} = 1.5 V	2.2 V		±1.1	±4	
		SREFx = 011, buffered external reference (see Note 1), V_{eREF+} = 2.5 V	3 V		±1.1	±3	
E_T	Total unadjusted error	SREFx = 010, unbuffered external reference, V_{eREF+} = 1.5 V	2.2 V		±2	±5	LSB
		SREFx = 010, unbuffered external reference, V_{eREF+} = 2.5 V	3 V		±2	±5	
		SREFx = 011, buffered external reference (see Note 1), V_{eREF+} = 1.5 V	2.2 V		±2	±7	
		SREFx = 011, buffered external reference (see Note 1), V_{eREF+} = 2.5 V	3 V		±2	±6	

NOTES: 1. The reference buffer offset adds to the gain and total unadjusted error.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

10-bit ADC, temperature sensor and built-in V_{MID}

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{SENSOR}	Temperature sensor supply current (see Note 1)	REFON = 0, INCHx = 0Ah, T_A = 25°C	2.2 V		40	120	μA
			3 V		60	160	
TC_{SENSOR}†		ADC10ON = 1, INCHx = 0Ah (see Note 2)	2.2 V/3 V	3.44	3.55	3.66	mV/°C
$V_{Offset,Sensor}$	Sensor offset voltage	ADC10ON = 1, INCHx = 0Ah (see Note 2)		−100		100	mV
V_{Sensor}	Sensor output voltage (see Note 3)	Temperature sensor voltage at T_A = 105°C (T version only)	2.2 V/3 V	1265	1365	1465	mV
		Temperature sensor voltage at T_A = 85°C	2.2 V/3 V	1195	1295	1395	
		Temperature sensor voltage at T_A = 25°C	2.2 V/3 V	985	1085	1185	
		Temperature sensor voltage at T_A = 0°C	2.2 V/3 V	895	995	1095	
$t_{Sensor(sample)}$	Sample time required if channel 10 is selected (see Note 4)	ADC10ON = 1, INCHx = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V/3 V	30			μs
I_{VMID}	Current into divider at channel 11 (see Note 5)	ADC10ON = 1, INCHx = 0Bh	2.2 V			NA	μA
			3 V			NA	
V_{MID}	V_{CC} divider at channel 11	ADC10ON = 1, INCHx = 0Bh, V_{MID} is ≈0.5 x V_{CC}	2.2 V	1.06	1.1	1.14	V
			3 V	1.46	1.5	1.54	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected (see Note 6)	ADC10ON = 1, INCHx = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V	1400			ns
			3 V	1220			

NOTES:
1. The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1), or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is included in I_{REF+}. When REFON = 0, I_{SENSOR} applies during conversion of the temperature sensor input (INCH = 0Ah).
2. The following formula can be used to calculate the temperature sensor output voltage:
   $V_{Sensor,typ} = TC_{Sensor}$ (273 + T [°C]) + $V_{Offset,sensor}$ [mV] or
   $V_{Sensor,typ} = TC_{Sensor}$ T [°C] + $V_{Sensor}(T_A = 0°C)$ [mV]
3. Results based on characterization and/or production test, not TC_{Sensor} or $V_{Offset,sensor}$.
4. The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
5. No additional current is needed. The V_{MID} is used during sampling.
6. The on time, $t_{VMID(on)}$, is included in the sampling time, $t_{VMID(sample)}$; no additional on time is needed.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

operational amplifier OA, supply specifications (MSP430x22x4 only)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range			2.2		3.6	V
I_{CC}	Supply current (see Note 1)	Fast Mode	2.2 V/3 V		180	290	µA
		Medium Mode			110	190	
		Slow Mode			50	80	
PSRR	Power supply rejection ratio	Non-inverting	2.2 V/3 V		70		dB

NOTES: 1. Corresponding pins configured as OA inputs and outputs respectively.

operational amplifier OA, input/output specifications (MSP430x22x4 only)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$V_{I/P}$	Input voltage range				−0.1		V_{CC}−1.2	V
I_{lkg}	Input leakage current (see Notes 1 and 2)	T_A = −40 to +55°C		2.2 V/3 V	−5	±0.5	5	nA
		T_A = +55 to +85°C			−20	±5	20	
		T_A = +85 to +105°C			−50		50	
V_n	Voltage noise density, I/P	Fast Mode	$f_{V(I/P)}$ = 1 kHz			50		nV/√Hz
		Medium Mode				80		
		Slow Mode				140		
		Fast Mode	$f_{V(I/P)}$ = 10 kHz			30		
		Medium Mode				50		
		Slow Mode				65		
V_{IO}	Offset voltage, I/P			2.2 V/3 V			±10	mV
	Offset temperature drift, I/P	see Note 3		2.2 V/3 V		±10		µV/°C
	Offset voltage drift with supply, I/P	0.3 V ≤ V_{IN} ≤ V_{CC}−1.0 V ΔV_{CC} ≤ ± 10%, T_A = 25°C		2.2 V/3 V			±1.5	mV/V
V_{OH}	High-level output voltage, O/P	Fast Mode, I_{SOURCE} ≤ −500 µA		2.2 V/3 V	V_{CC}−0.2		V_{CC}	V
		Slow Mode, I_{SOURCE} ≤ −150 µA			V_{CC}−0.1		V_{CC}	
V_{OL}	Low-level output voltage, O/P	Fast Mode, I_{SOURCE} ≤ +500 µA		2.2 V/3 V	V_{SS}		0.2	V
		Slow Mode, I_{SOURCE} ≤ +150 µA			V_{SS}		0.1	
$R_{O/P(OAx)}$	Output resistance (see Figure 25 and Note 4)	R_{Load}= 3 kΩ, C_{Load} = 50pF, $V_{O/P(OAx)}$ < 0.2 V		2.2 V/3 V		150	250	Ω
		R_{Load}= 3 kΩ, C_{Load} = 50pF, $V_{O/P(OAx)}$ > V_{CC} − 1.2 V				150	250	
		R_{Load}= 3 kΩ, C_{Load} = 50pF, 0.2 V ≤ $V_{O/P(OAx)}$ ≤ V_{CC} − 0.2 V				0.1	4	
CMRR	Common-mode rejection ratio	Noninverting		2.2 V/3 V		70		dB

NOTES: 1. ESD damage can degrade input current leakage.
2. The input bias current is overridden by the input leakage current.
3. Calculated using the box method
4. Specification valid for voltage-follower OAx configuration

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

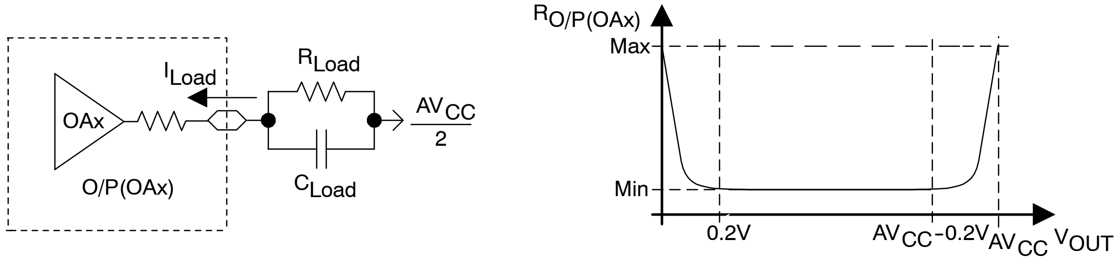


Figure 25. OAx Output Resistance Tests

operational amplifier OA, dynamic specifications (MSP430x22x4 only)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
SR	Slew rate	Fast Mode			1.2		V/µs
		Medium Mode			0.8		
		Slow Mode			0.3		
	Open-loop voltage gain				100		dB
ϕ_m	Phase margin	C_L = 50 pF			60		deg
	Gain margin	C_L = 50 pF			20		dB
GBW	Gain-bandwidth product (see Figure 26 and Figure 27)	Noninverting, Fast Mode, R_L = 47 kΩ, C_L = 50 pF	2.2 V/3 V		2.2		MHz
		Noninverting, Medium Mode, R_L =300 kΩ, C_L = 50pF			1.4		
		Non-inverting, Slow Mode, R_L =300 kΩ, C_L = 50pF			0.5		
$t_{en(on)}$	Enable time on	t_{on}, Noninverting, Gain = 1	2.2 V/3 V		10	20	µs
$t_{en(off)}$	Enable time off		2.2 V/3 V			1	µs

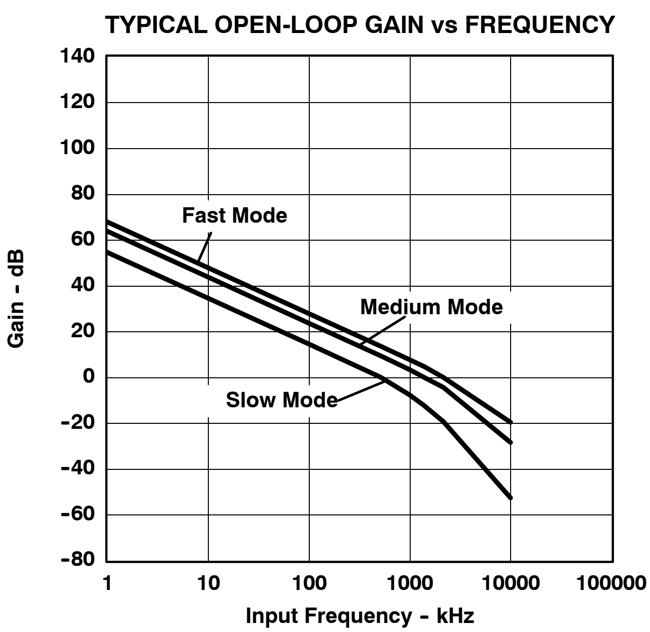


Figure 26

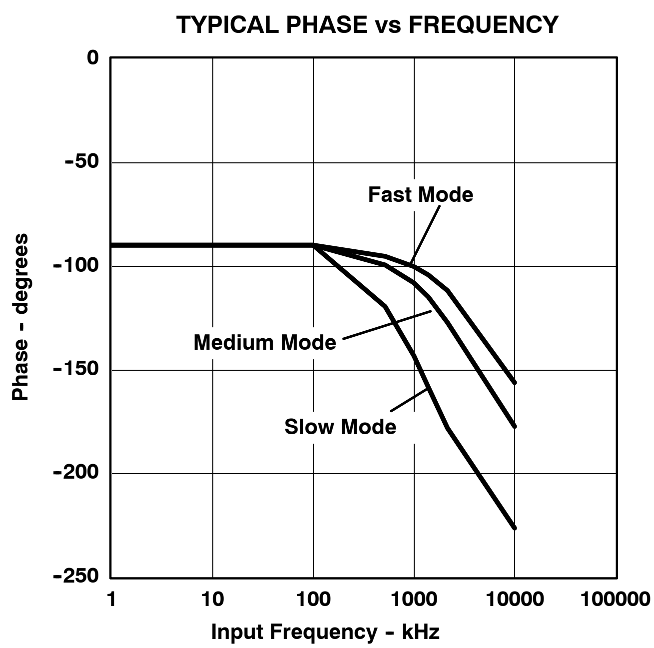


Figure 27

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

operational amplifier OA feedback network, resistor network (MSP430x22x4 only) (see Note 1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
R_{total}	Total resistance of resistor string			76	96	128	kΩ
R_{unit}	Unit resistor of resistor string (see Note 2)			4.8	6	8	kΩ

NOTES: 1. A single resistor string is composed of 4 R_{unit} + 4 R_{unit} + 2 R_{unit} + 2 R_{unit} + 1 R_{unit} + 1 R_{unit} + 1 R_{unit} + 1 R_{unit} = 16 R_{unit} = R_{total}.
2. For the matching (i.e. the relative accuracy) of the unit resistors on a device refer to the gain and level specifications of the respective configurations.

operational amplifier OA feedback network, comparator mode (OAFCx = 3) (MSP430x22x4 only)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{Level}	Comparator level	OAFBRx = 1, OARRIP = 0	2.2 V/ 3 V	0.245	1/4	0.255	V_{CC}
		OAFBRx = 2, OARRIP = 0		0.495	1/2	0.505	
		OAFBRx = 3, OARRIP = 0		0.619	5/8	0.631	
		OAFBRx = 4, OARRIP = 0			N/A (see Note 1)		
		OAFBRx = 5, OARRIP = 0			N/A (see Note 1)		
		OAFBRx = 6, OARRIP = 0			N/A (see Note 1)		
		OAFBRx = 7, OARRIP = 0			N/A (see Note 1)		
		OAFBRx = 1, OARRIP = 1		0.061	1/16	0.065	
		OAFBRx = 2, OARRIP = 1		0.122	1/8	0.128	
		OAFBRx = 3, OARRIP = 1		0.184	3/16	0.192	
		OAFBRx = 4, OARRIP = 1		0.245	1/4	0.255	
		OAFBRx = 5, OARRIP = 1		0.367	3/8	0.383	
		OAFBRx = 6, OARRIP = 1		0.495	1/2	0.505	
		OAFBRx = 7, OARRIP = 1			N/A (see Note 1)		
t_{PLH}, t_{PHL}	Propagation delay (low-high and high-low)	Fast Mode, Overdrive 10 mV	2.2 V/ 3 V		40		µs
		Fast Mode, Overdrive 100 mV			4		
		Fast Mode, Overdrive 500 mV			3		
		Medium Mode, Overdrive 10 mV			60		
		Medium Mode, Overdrive 100 mV			6		
		Medium Mode, Overdrive 500 mV			5		
		Slow Mode, Overdrive 10 mV			160		
		Slow Mode, Overdrive 100 mV			20		
		Slow Mode, Overdrive 500 mV			15		

NOTES: 1. The level is not available due to the analog input voltage range of the operational amplifier.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

operational amplifier OA feedback network, noninverting amplifier mode (OAFCx = 4) (MSP430x22x4 only)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
G	Gain	OAFBRx = 0	2.2 V/ 3 V	0.998	1.00	1.002	
		OAFBRx = 1		1.328	1.334	1.340	
		OAFBRx = 2		1.985	2.001	2.017	
		OAFBRx = 3		2.638	2.667	2.696	
		OAFBRx = 4		3.94	4.00	4.06	
		OAFBRx = 5		5.22	5.33	5.44	
		OAFBRx = 6		7.76	7.97	8.18	
		OAFBRx = 7		15.0	15.8	16.6	
THD	Total harmonic distortion/ nonlinearity	All gains	2.2 V		−60		dB
			3 V		−70		
t_{Settle}	Settling time (see Note 1)	All power modes	2.2 V/3 V		7	12	µs

NOTES: 1. The settling time specifies the time until an ADC result is stable. This includes the minimum required sampling time of the ADC. The settling time of the amplifier itself might be faster.

operational amplifier OA feedback network, inverting amplifier mode (OAFCx = 6) (MSP430x22x4 only) (see Note 1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
G	Gain	OAFBRx = 1	2.2 V/ 3 V	−0.345	−0.335	−0.325	
		OAFBRx = 2		−1.023	−1.002	−0.979	
		OAFBRx = 3		−1.712	−1.668	−1.624	
		OAFBRx = 4		−3.10	−3.00	−2.90	
		OAFBRx = 5		−4.51	−4.33	−4.15	
		OAFBRx = 6		−7.37	−6.97	−6.57	
		OAFBRx = 7		−16.3	−14.8	−13.1	
THD	Total harmonic distortion/ nonlinearity	All gains	2.2 V		−60		dB
			3 V		−70		
t_{Settle}	Settling time (see Note 2)	All power modes	2.2 V/3 V		7	12	µs

NOTES: 1. This includes the 2 OA configuration “inverting amplifier with input buffer”. Both OA needs to be set to the same power mode OAPMx.
2. The settling time specifies the time until an ADC result is stable. This includes the minimum required sampling time of the ADC. The settling time of the amplifier itself might be faster.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

flash memory

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and erase supply voltage			2.2		3.6	V
f_{FTG}	Flash timing generator frequency			257		476	kHz
I_{PGM}	Supply current from V_{CC} during program		2.2 V/3.6 V		1	5	mA
I_{ERASE}	Supply current from V_{CC} during erase		2.2 V/3.6 V		1	7	mA
t_{CPT}	Cumulative program time (see Note 1)		2.2 V/3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time		2.2 V/3.6 V	20			ms
	Program/erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	see Note 2			30		t_{FTG}
$t_{Block, 0}$	Block program time for first byte or word	see Note 2			25		t_{FTG}
$t_{Block, 1-63}$	Block program time for each additional byte or word	see Note 2			18		t_{FTG}
$t_{Block, End}$	Block program end-sequence wait time	see Note 2			6		t_{FTG}
$t_{Mass Erase}$	Mass erase time	see Note 2			10593		t_{FTG}
$t_{Seg Erase}$	Segment erase time	see Note 2			4819		t_{FTG}

NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. These values are hardwired into the flash controller's state machine ($t_{FTG} = 1/f_{FTG}$).

RAM

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(RAMh)}$	RAM retention supply voltage (see Note 1)	CPU halted	1.6			V

NOTE 1: This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

JTAG and Spy-Bi-Wire interface

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency		2.2 V / 3 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse length		2.2 V / 3 V	0.025		15	µs
$t_{SBW,En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge, see Note 1)		2.2 V/ 3 V			1	µs
$t_{SBW,Ret}$	Spy-Bi-Wire return to normal operation time		2.2 V/ 3 V	15		100	µs
f_{TCK}	TCK input frequency (see Note 2)		2.2 V	0		5	MHz
			3 V	0		10	
$R_{Internal}$	Internal pull-down resistance on TEST		2.2 V/ 3 V	25	60	90	kΩ

NOTES: 1. Tools accessing the Spy-Bi-Wire interface need to wait for the maximum $t_{SBW,En}$ time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.
2. f_{TCK} may be restricted to meet the timing requirements of the module selected.

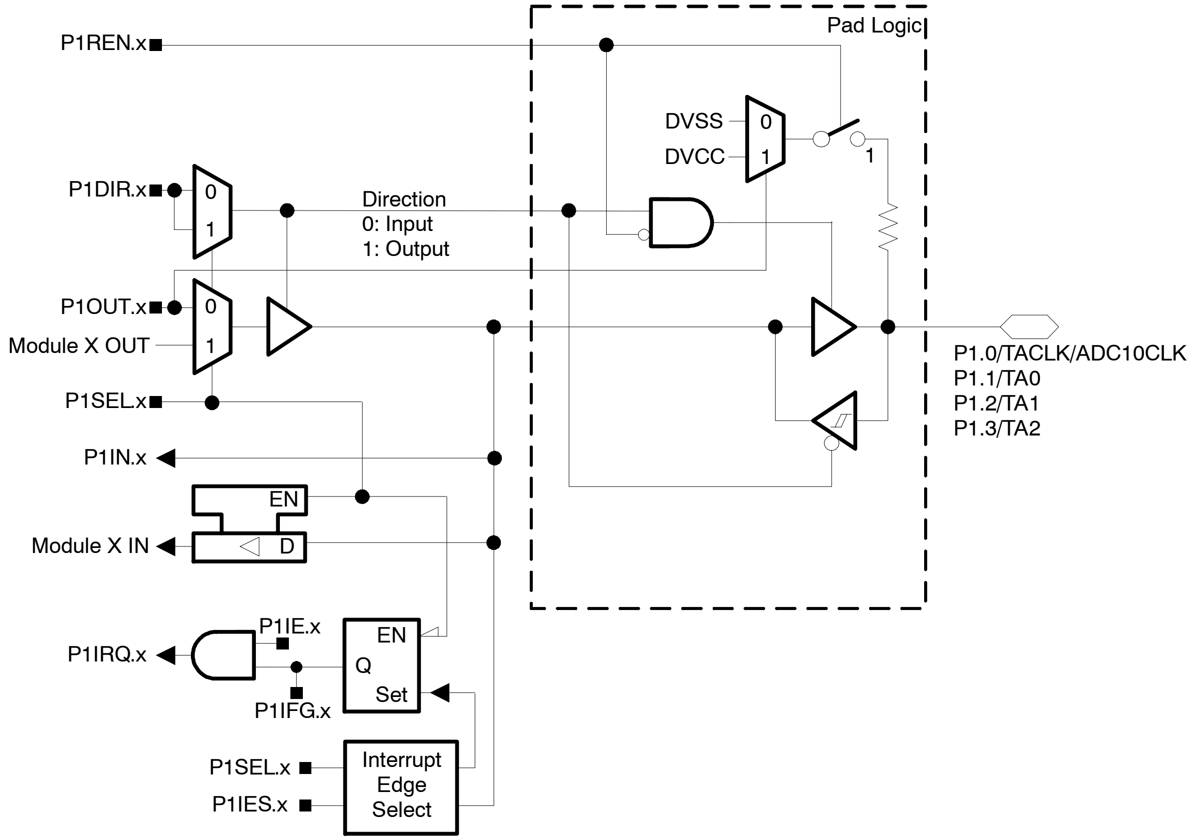
JTAG fuse (see Note 1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C		2.5			V
V_{FB}	Voltage level on TEST for fuse blow			6		7	V
I_{FB}	Supply current into TEST during fuse blow					100	mA
t_{FB}	Time to blow fuse					1	ms

NOTES: 1. Once the fuse is blown, no further access to the JTAG/Test and emulation feature is possible, and it is switched to bypass mode.

APPLICATION INFORMATION

Port P1 pin schematic: P1.0 to P1.3, input/output with Schmitt trigger



Port P1 (P1.0 to P1.3) pin functions

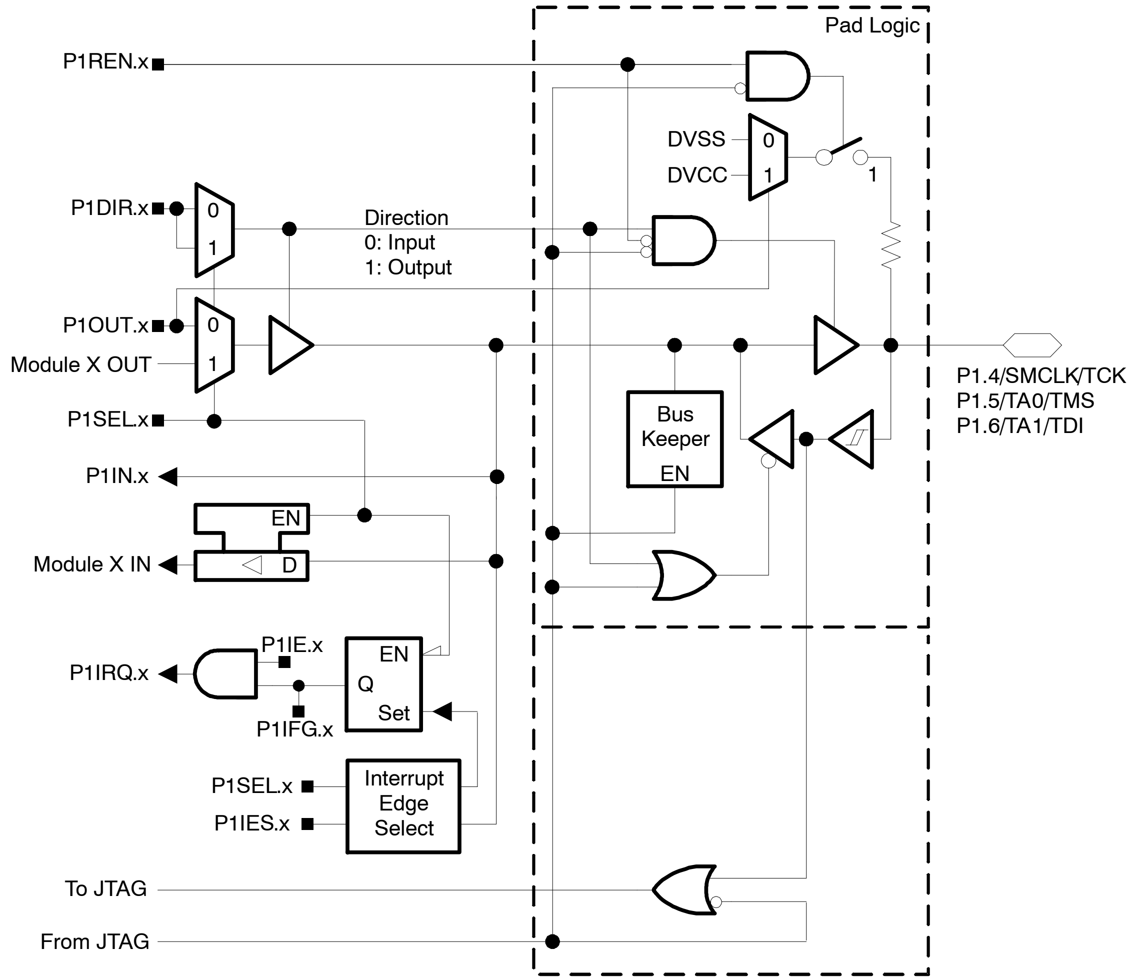
PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/ TACLK/ADC10CLk	0	P1.0† (I/O)	I: 0; O: 1	0
		Timer_A3.TACLK	0	1
		ADC10CLK	1	1
P1.1/TA0	1	P1.1† (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.2/TA1	2	P1.2† (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.3/TA2	3	P1.3† (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable

2. X: Don’t care

Port P1 pin schematic: P1.4 to P1.6, input/output with Schmitt trigger and in-system access features



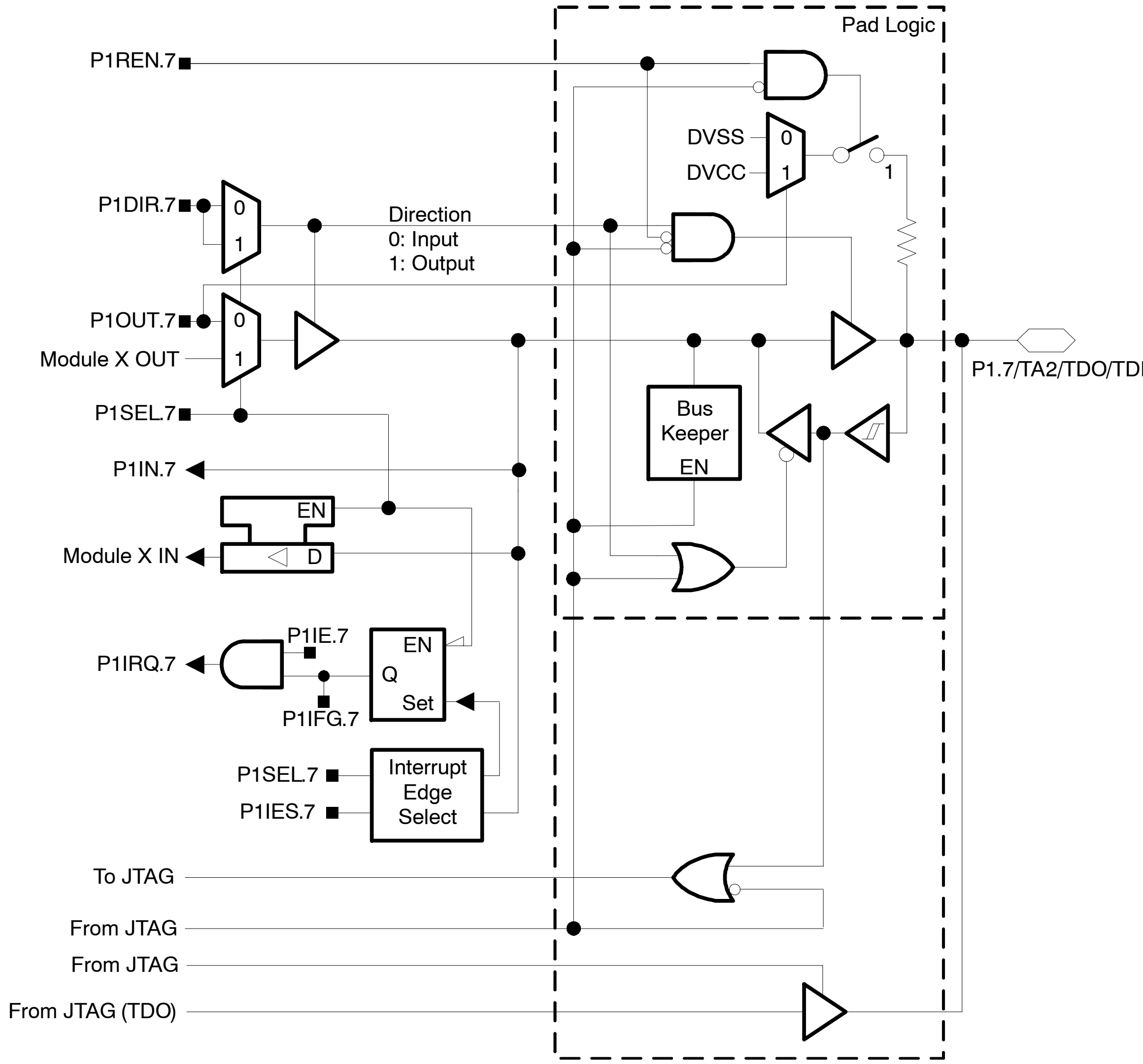
Port P1 (P1.4 to P1.6) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P1DIR.x	P1SEL.x	4-Wire JTAG
P1.4/SMCLK/TCK	4	P1.4† (I/O)	I: 0; O: 1	0	0
		SMCLK	1	1	0
		TCK	X	X	1
P1.5/TA0/TMS	5	P1.5† (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA0	1	1	0
		TMS	X	X	1
P1.6/TA1/TDI/TCLK	6	P1.6† (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA1	1	1	0
		TDI/TCLK (see Note 3)	X	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable
2. X: Don't care
3. Function controlled by JTAG.

Port P1 pin schematic: P1.7, input/output with Schmitt trigger and in-system access features



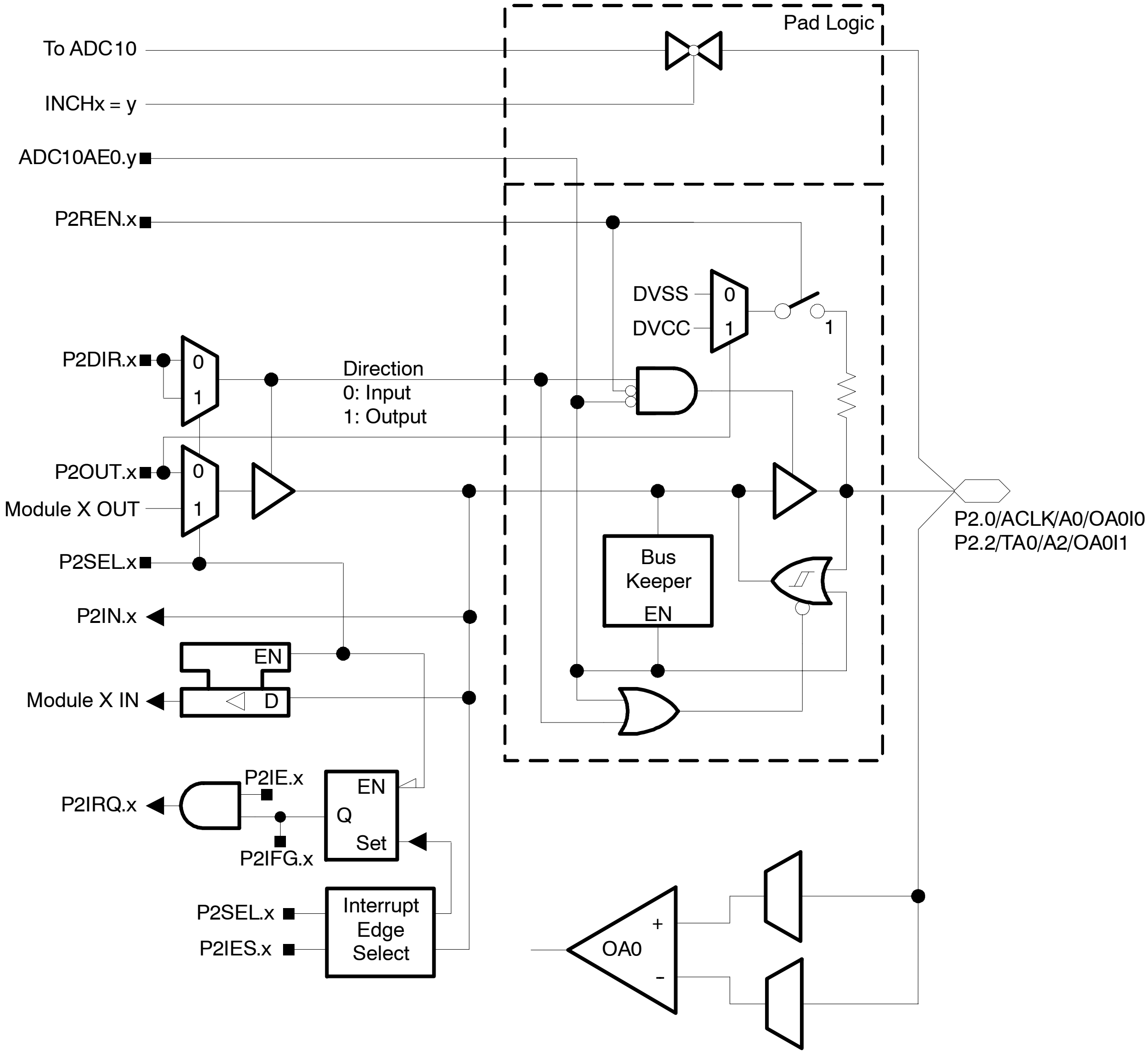
Port P1 (P1.7) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P1DIR.x	P1SEL.x	4-Wire JTAG
P1.7/TA2/TDO/TDI	7	P1.7† (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA2	1	1	0
		TDO/TDI (see Note 3)	X	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable
2. X: Don't care
3. Function controlled by JTAG.

Port P2 pin schematic: P2.0, P2.2, input/output with Schmitt trigger



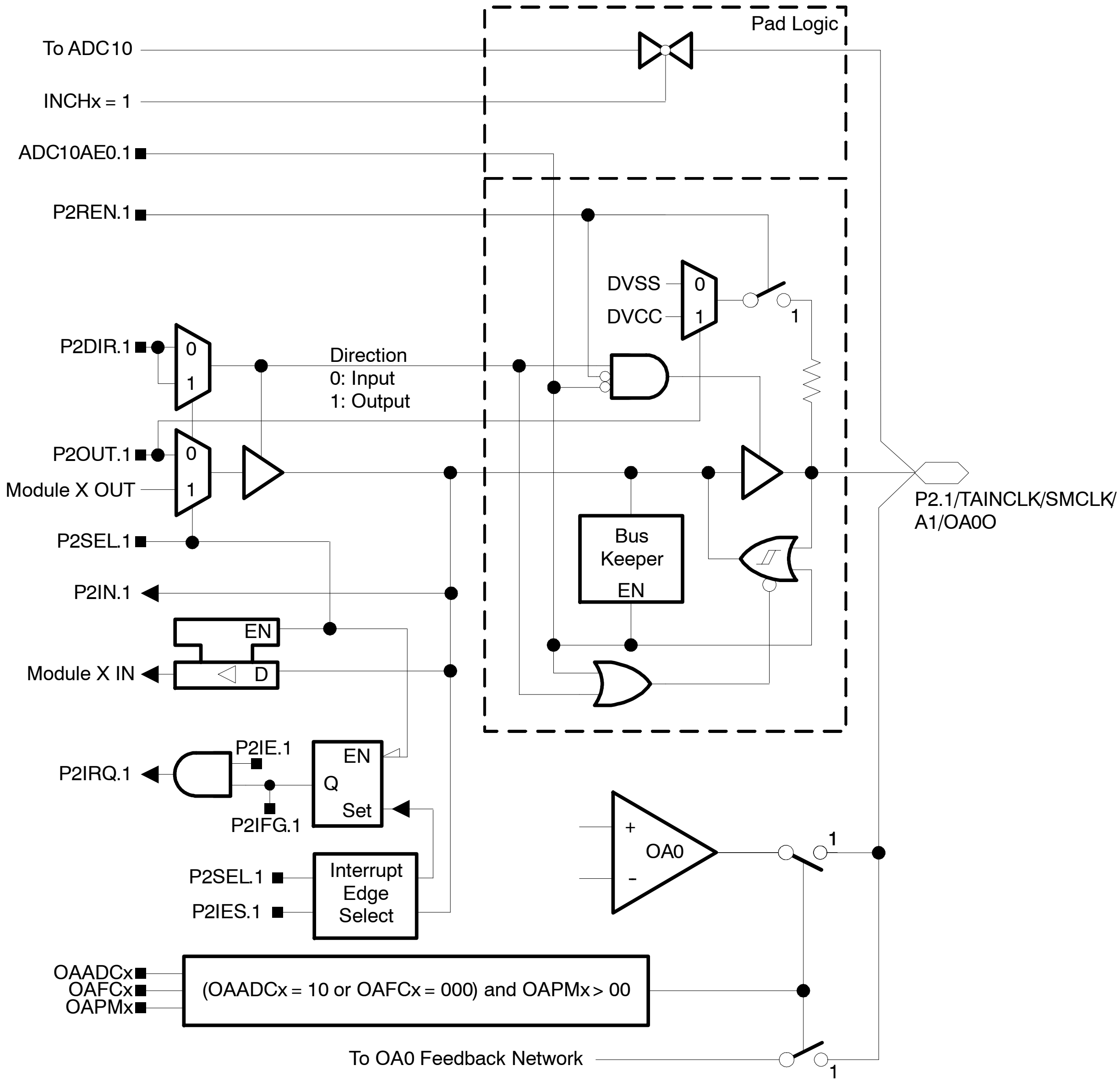
Port P2 (P2.0, P2.2) pin functions

PIN NAME (P2.X)	X	Y	FUNCTION	CONTROL BITS / SIGNALS		
				P2DIR.x	P2SEL.x	ADC10AE0.y
P2.0/ACLK/A0/OA0I0	0	0	P2.0† (I/O)	I: 0; O: 1	0	0
			ACLK	1	1	0
			A0/OA0I0 (see Note 3)	X	X	1
P2.2/TA0/A2/OA0I1	2	2	P2.2† (I/O)	I: 0; O: 1	0	0
			Timer_A3.CCI0B	0	1	0
			Timer_A3.TA0	1	1	0
			A2/OA0I1 (see Note 3)	X	X	1

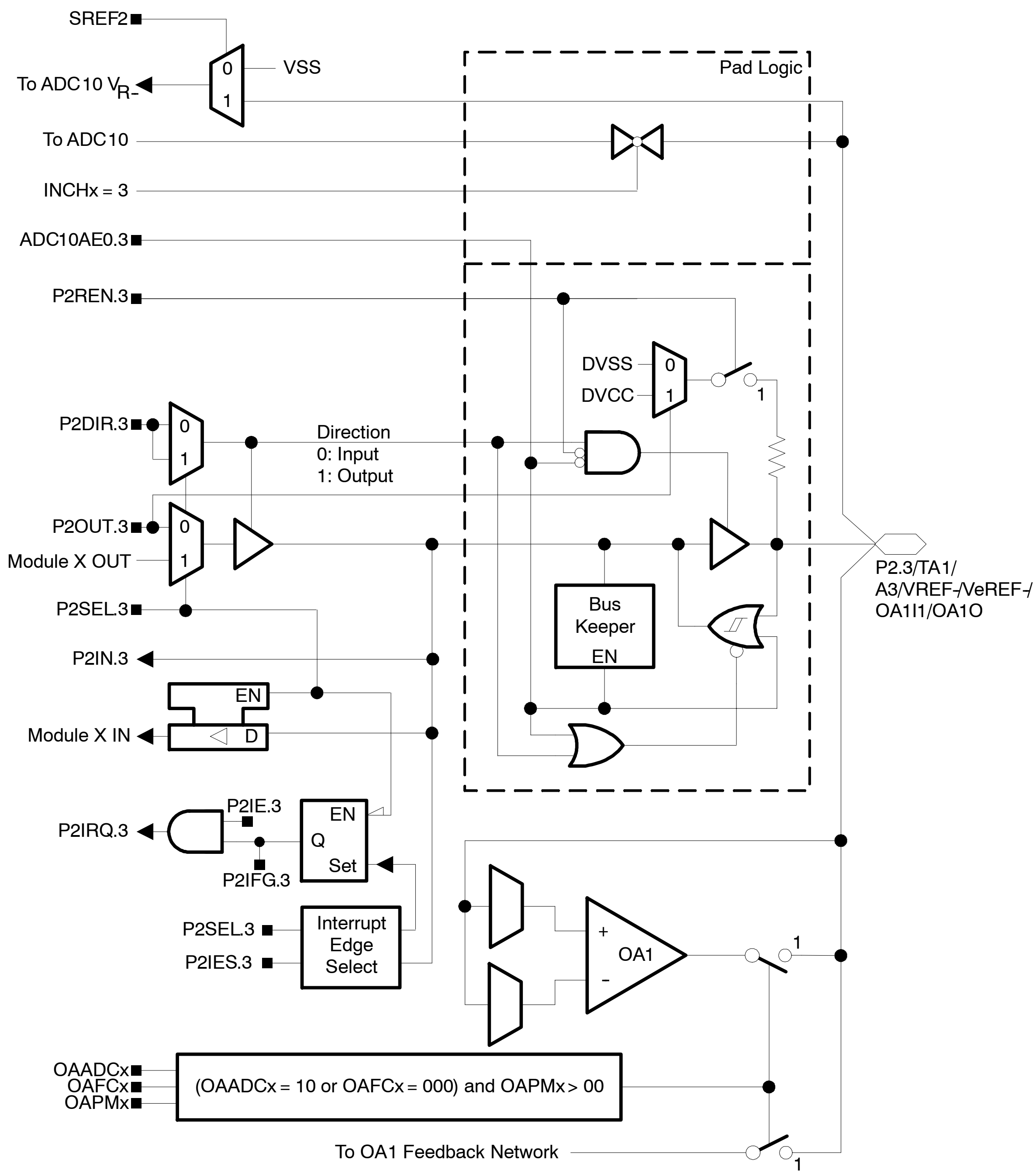
† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable
2. X: Don't care
3. Setting the ADC10AE0.y bit disables the output driver as well as the input schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P2 pin schematic: P2.1, input/output with Schmitt trigger



Port P2 pin schematic: P2.3, input/output with Schmitt trigger



Port P2 (P2.1) pin functions

PIN NAME (P2.X)	X	Y	FUNCTION	CONTROL BITS / SIGNALS		
				P2DIR.x	P2SEL.x	ADC10AE0.y
P2.1/TAINCLK/SMCLK /A1/OA0O	1	1	P2.1† (I/O)	I: 0; O: 1	0	0
			Timer_A3.INCLK	0	1	0
			SMCLK	1	1	0
			A1/OA0O (see Note 3)	X	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable
2. X: Don't care
3. Setting the ADC10AE0.y bit disables the output driver as well as the input schmitt trigger to prevent parasitic cross currents when applying analog signals.

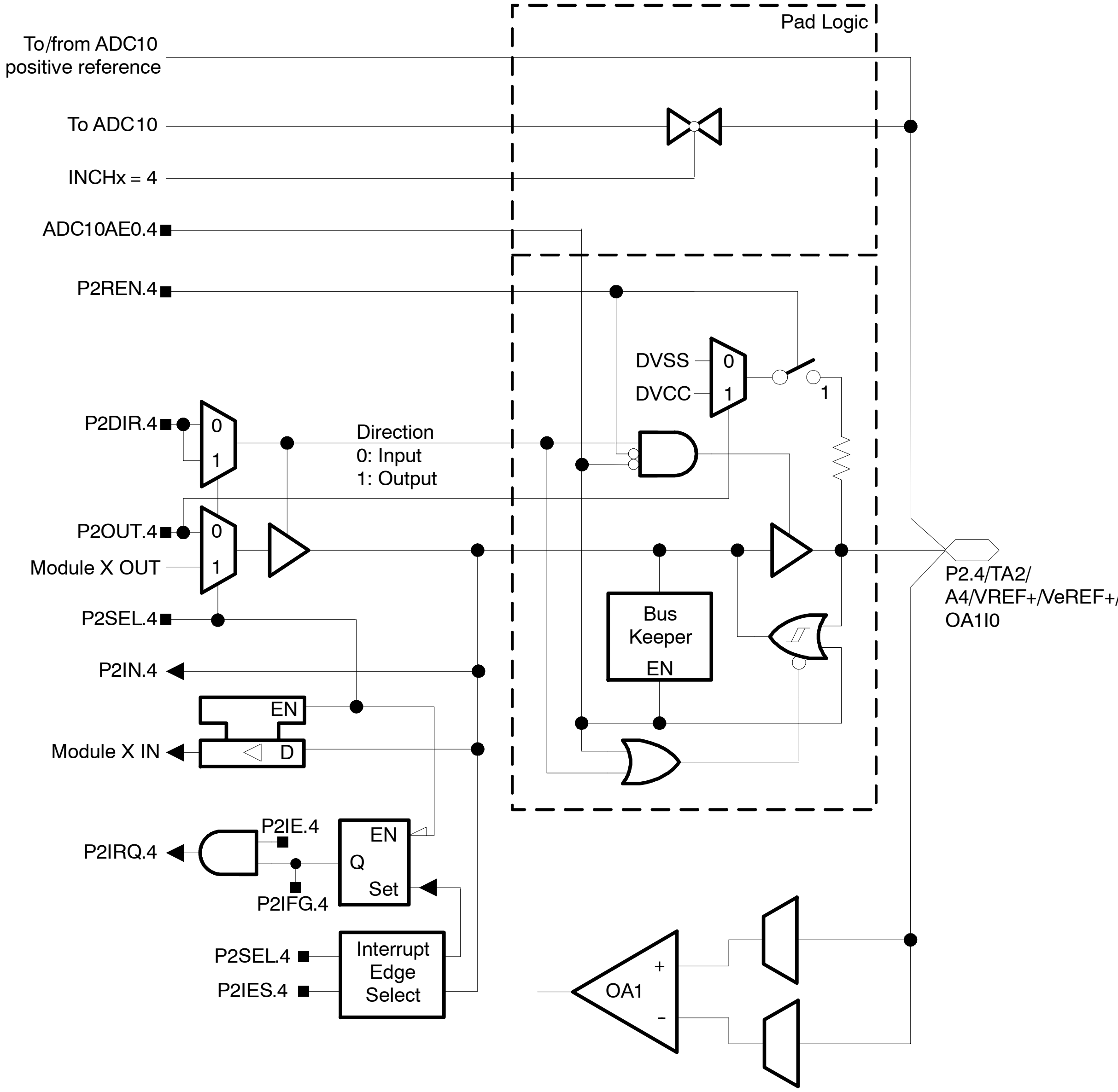
Port P2 (P2.3) pin functions

PIN NAME (P2.X)	X	Y	FUNCTION	CONTROL BITS / SIGNALS		
				P2DIR.x	P2SEL.x	ADC10AE0.y
P2.3/TA1/ A3/V_{REF-}/V_{eREF-}/ OA1I1/OA1O	3	3	P2.3† (I/O)	I: 0; O: 1	0	0
			Timer_A3.CCI1B	0	1	0
			Timer_A3.TA1	1	1	0
			A3/V_{REF-}/V_{eREF-}/OA1I1/OA1O (see Note 3)	X	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable
2. X: Don't care
3. Setting the ADC10AE0.y bit disables the output driver as well as the input schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P2 pin schematic: P2.4, input/output with Schmitt trigger



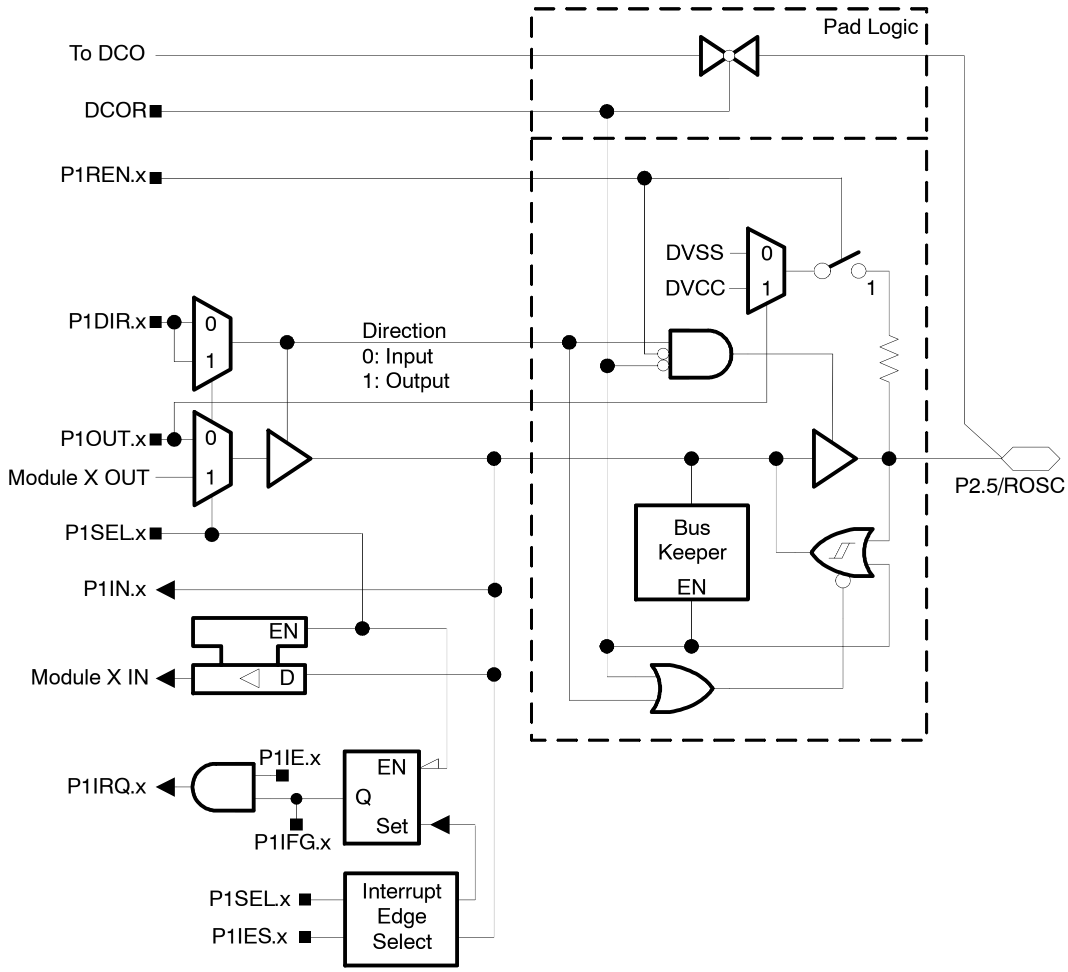
Port P2 (P2.4) pin functions

PIN NAME (P2.X)	X	Y	FUNCTION	CONTROL BITS / SIGNALS		
				P2DIR.x	P2SEL.x	ADC10AE0.y
P2.4/TA2/ A4/V_{REF+}/V_{eREF+}/ OA1I0	4	4	P2.4† (I/O)	I: 0; O: 1	0	0
			Timer_A3.TA2	1	1	0
			A4/V_{REF+}/V_{eREF+}/OA1I0 (see Note 3)	X	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable
2. X: Don't care
3. Setting the ADC10AE0.y bit disables the output driver as well as the input schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P2 pin schematic: P2.5, input/output with Schmitt trigger and external R_{OSC} for DCO



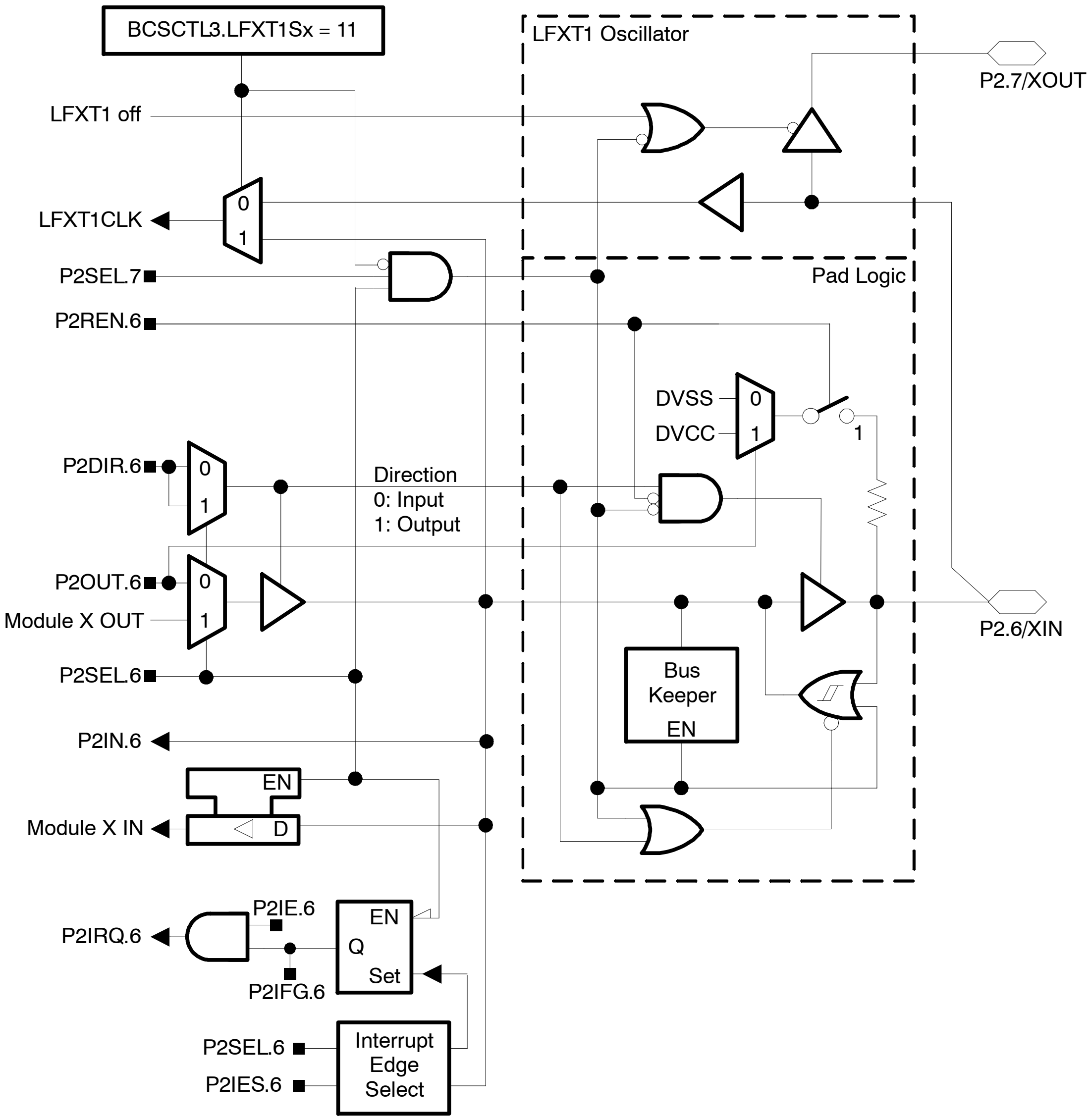
Port P2 (P2.5) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P2DIR.x	P2SEL.x	DCOR
P2.5/R_{OSC}	5	P2.5† (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DV_{SS}	1	1	0
		R_{OSC}	X	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable
2. X: Don't care
3. Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P2 pin schematic: P2.6, input/output with Schmitt trigger and crystal oscillator input



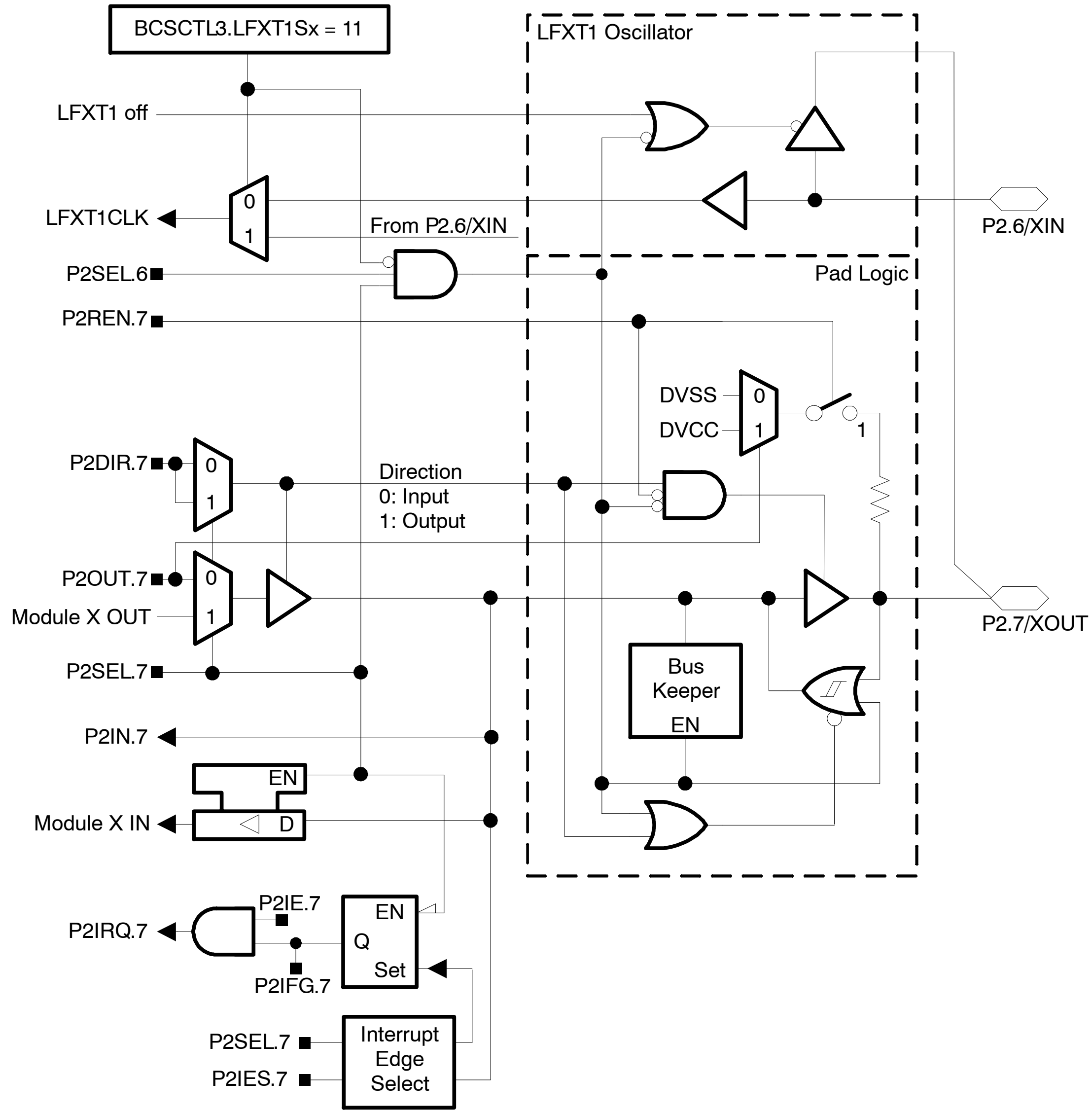
Port P2 (P2.6) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P2DIR.x	P2SEL.x
P2.6/XIN	6	P2.6 (I/O)	I: 0; O: 1	0
		XIN†	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable
2. X: Don't care

Port P2 pin schematic: P2.7, input/output with Schmitt trigger and crystal oscillator output



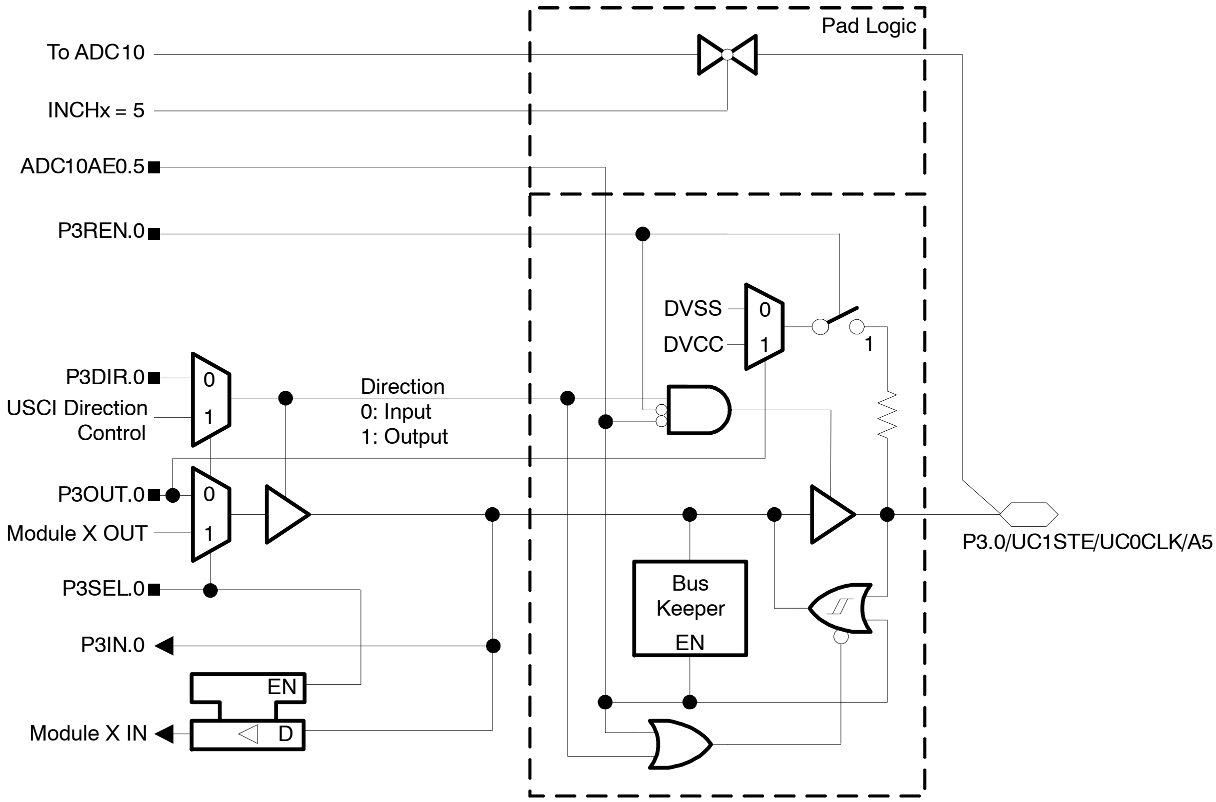
Port P2 (P2.7) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P2DIR.x	P2SEL.x
XOUT/P2.7	6	P2.7 (I/O)	I: 0; O: 1	0
		XOUT† (see Note 3)	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable
2. X: Don’t care
3. If the pin XOUT/P2.7 is used as an input a current can flow until P2SEL.7 is cleared due to the oscillator output driver connection to this pin after reset.

Port P3 pin schematic: P3.0, input/output with Schmitt trigger



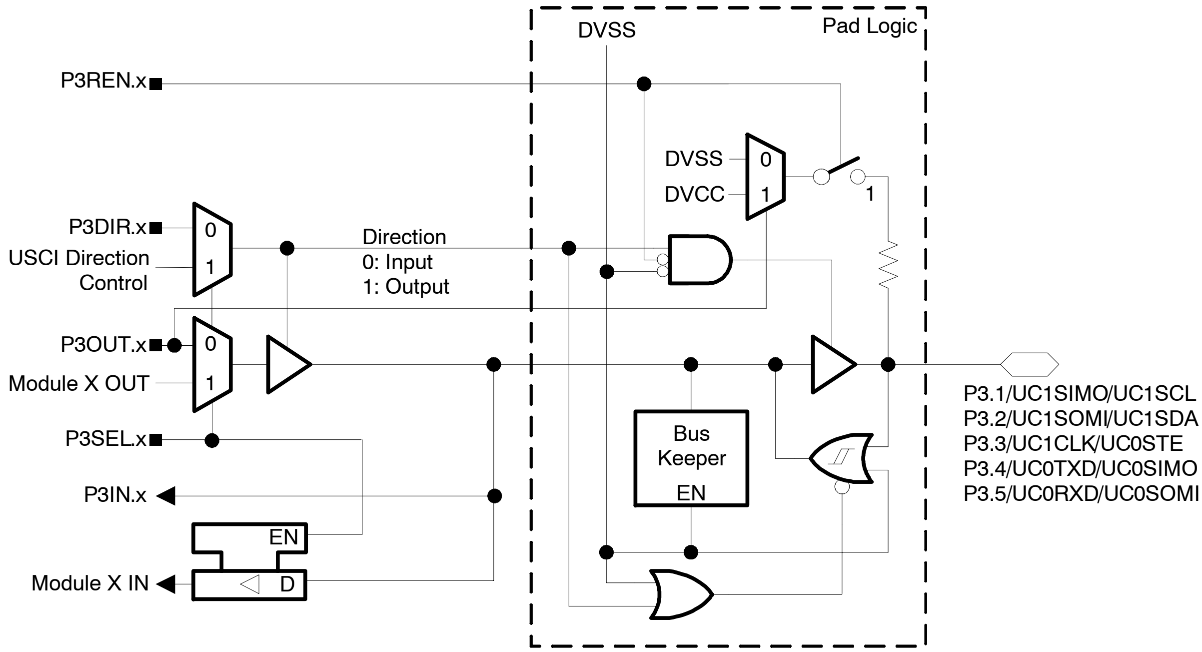
Port P3 (P3.0) pin functions

PIN NAME (P3.X)	X	Y	FUNCTION	CONTROL BITS / SIGNALS		
				P3DIR.x	P3SEL.x	ADC10AE0.y
P3.0/ UC1STE/UC0CLK/A5	0	5	P3.0† (I/O)	I: 0; O: 1	0	0
			UC1STE/UC0CLK (see Notes 3, 4)	X	1	0
			A5 (see Note 5)	X	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable
2. X: Don't care
3. The pin direction is controlled by the USCI module.
4. UC0CLK function takes precedence over UC1STE function. If the pin is required as UC0CLK input or output USCI1 will be forced to 3-wire SPI mode if 4-wire SPI mode is selected.
5. Setting the ADC10AE0.y bit disables the output driver as well as the input schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P3 pin schematic: P3.1 to P3.5, input/output with Schmitt trigger



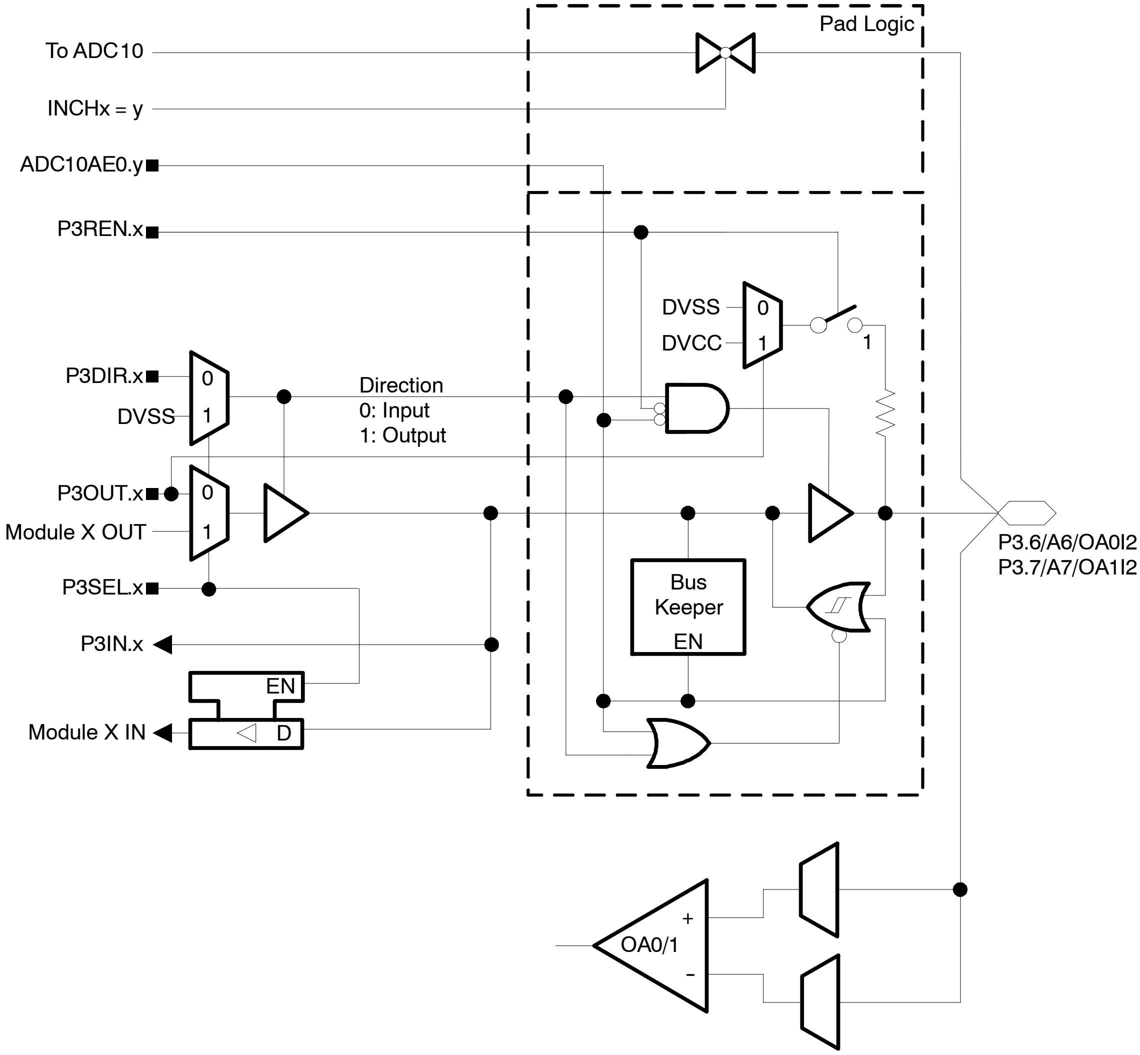
Port P3 (P3.1 to P3.5) pin functions

PIN NAME (P3.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P3DIR.x	P3SEL.x
P3.1/ UC1SIMO/UC1SDA	1	P3.1† (I/O)	I: 0; O: 1	0
		UC1SIMO/UC1SDA (see Note 3)	X	1
P3.2/ UC1SOMI/UC1SCL	1	P3.2† (I/O)	I: 0; O: 1	0
		UC1SOMI/UC1SCL (see Note 3)	X	1
P3.3/ UC1CLK/UC0STE	1	P3.3† (I/O)	I: 0; O: 1	0
		UC1CLK/UC0STE (see Notes 3, 4)	X	1
P3.4/ UC0TXD/UC0SIMO	1	P3.4† (I/O)	I: 0; O: 1	0
		UC0TXD/UC0SIMO (see Note 3)	X	1
P3.5/ UC0RXD/UC0SOMI	1	P3.5† (I/O)	I: 0; O: 1	0
		UC0RXD/UC0SOMI (see Note 3)	X	1

† Default after reset (PUC/POR)

NOTES:
1. N/A: Not available or not applicable
2. X: Don't care
3. The pin direction is controlled by the USCI module.
4. UC1CLK function takes precedence over UC0STE function. If the pin is required as UC1CLK input or output USCI0 will be forced to 3-wire SPI mode even if 4-wire SPI mode is selected.

Port P3 pin schematic: P3.6 to P3.7, input/output with Schmitt trigger



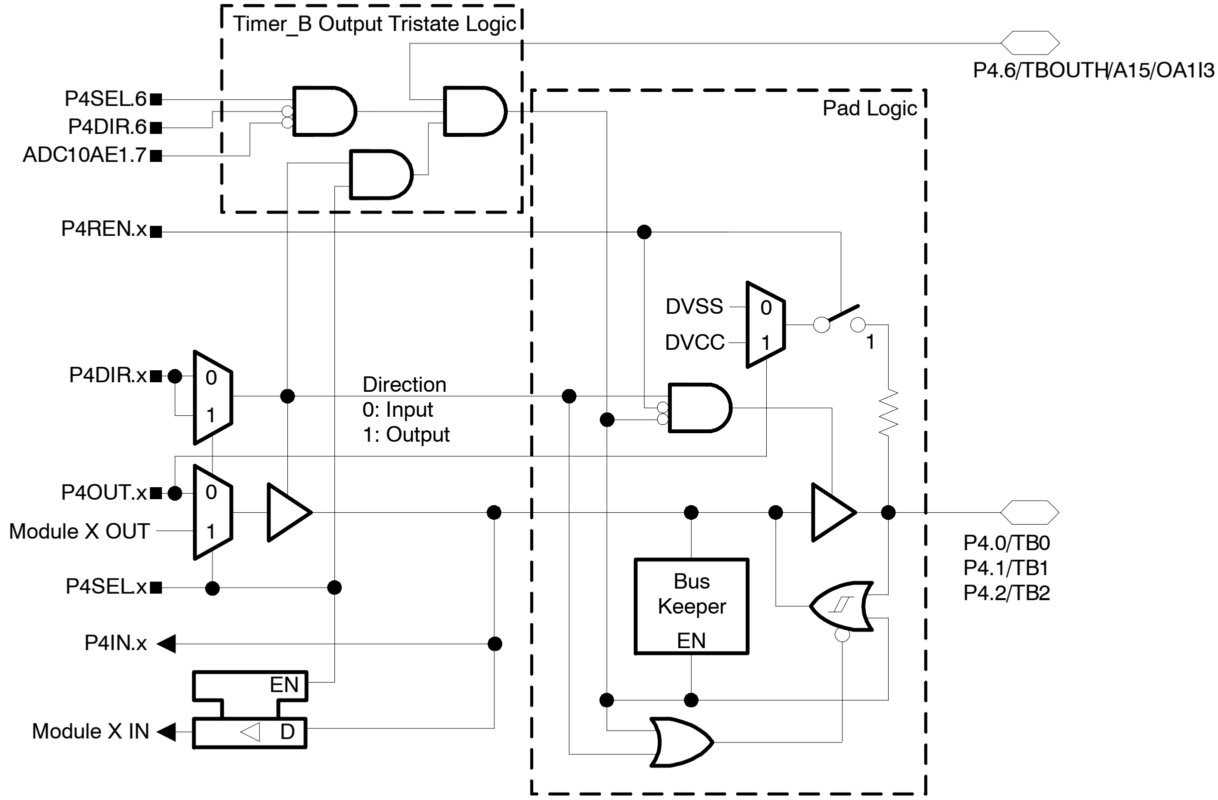
Port P3 (P3.6, P3.7) pin functions

PIN NAME (P3.X)	X	Y	FUNCTION	CONTROL BITS / SIGNALS		
				P3DIR.x	P3SEL.x	ADC10AE0.y
P3.6/A6/OA0I2	6	6	P3.6† (I/O)	I: 0; O: 1	0	0
			A6/OA0I2 (see Note 5)	X	X	1
P3.7/A7/OA1I2	7	7	P3.7† (I/O)	I: 0; O: 1	0	0
			A7/OA1I2 (see Note 5)	X	X	1

† Default after reset (PUC/POR)

NOTES:
1. N/A: Not available or not applicable
2. X: Don't care
3. The pin direction is controlled by the USCI module.
4. UC1CLK function takes precedence over UC0STE function. If the pin is required as UC1CLK input or output USCI0 will be forced to 3-wire SPI mode if 4-wire SPI mode is selected.
5. Setting the ADC10AE0.y bit disables the output driver as well as the input schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P4 pin schematic: P4.0 to P4.2, input/output with Schmitt trigger



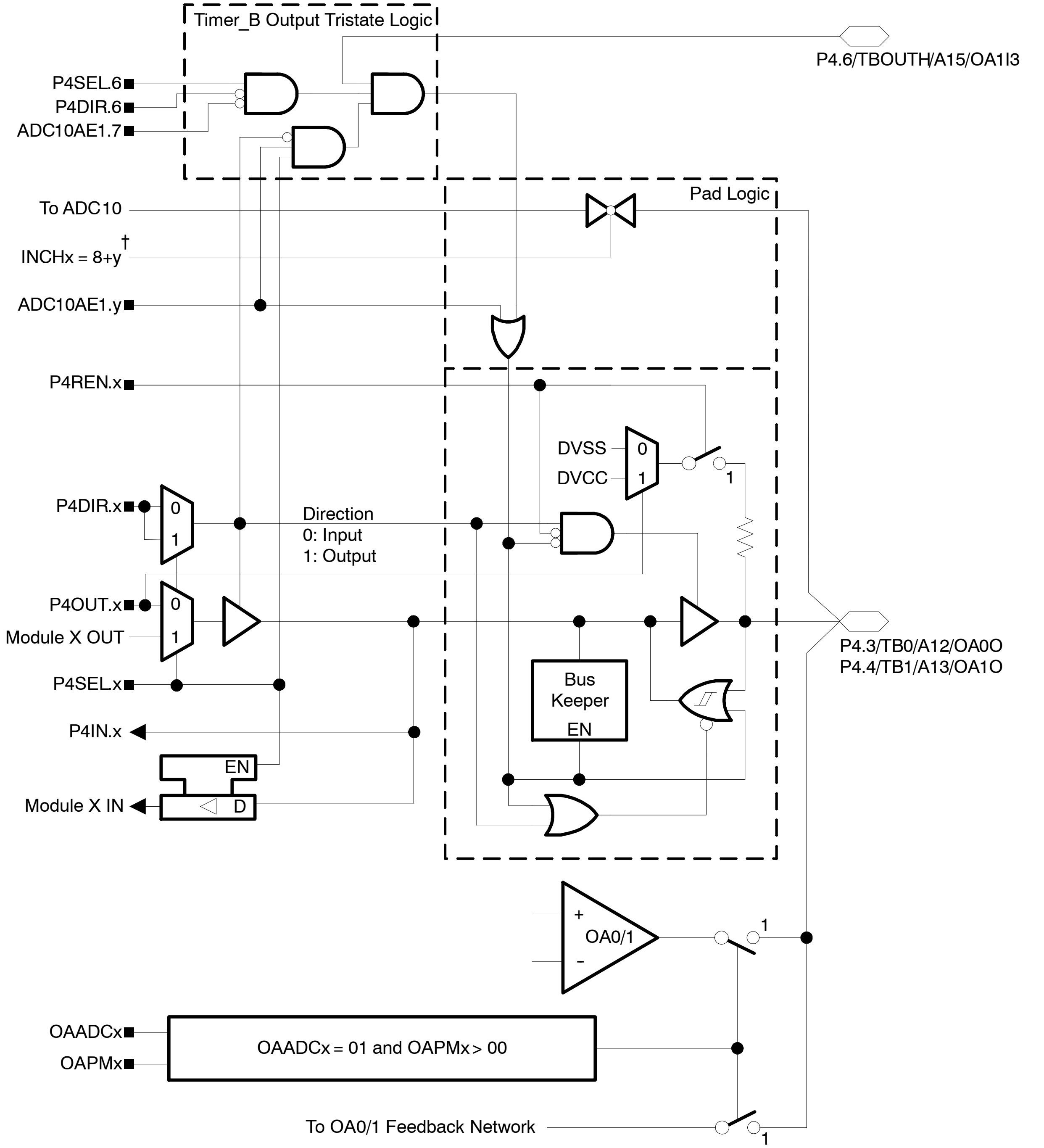
Port P4 (P4.0 to P4.2) pin functions

PIN NAME (P4.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P4DIR.x	P4SEL.x
P4.0/TB0	0	P4.0† (I/O)	I: 0; O: 1	0
		Timer_B3.CCI0A	0	1
		Timer_B3.TB0	1	1
P4.1/TB1	1	P4.1† (I/O)	I: 0; O: 1	0
		Timer_B3.CCI1A	0	1
		Timer_B3.TB1	1	1
P4.2/TB2	2	P4.2† (I/O)	I: 0; O: 1	0
		Timer_B3.CCI2A	0	1
		Timer_B3.TB2	1	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable
2. X: Don't care

Port P4 pin schematic: P4.3 to P4.4, input/output with Schmitt trigger



† If OAADCx = 11 and not OAFCx = 000 the ADC input A12 or A13 is internally connected to the OA0 or OA1 output respectively and the connections from the ADC and the operational amplifiers to the pad are disabled.

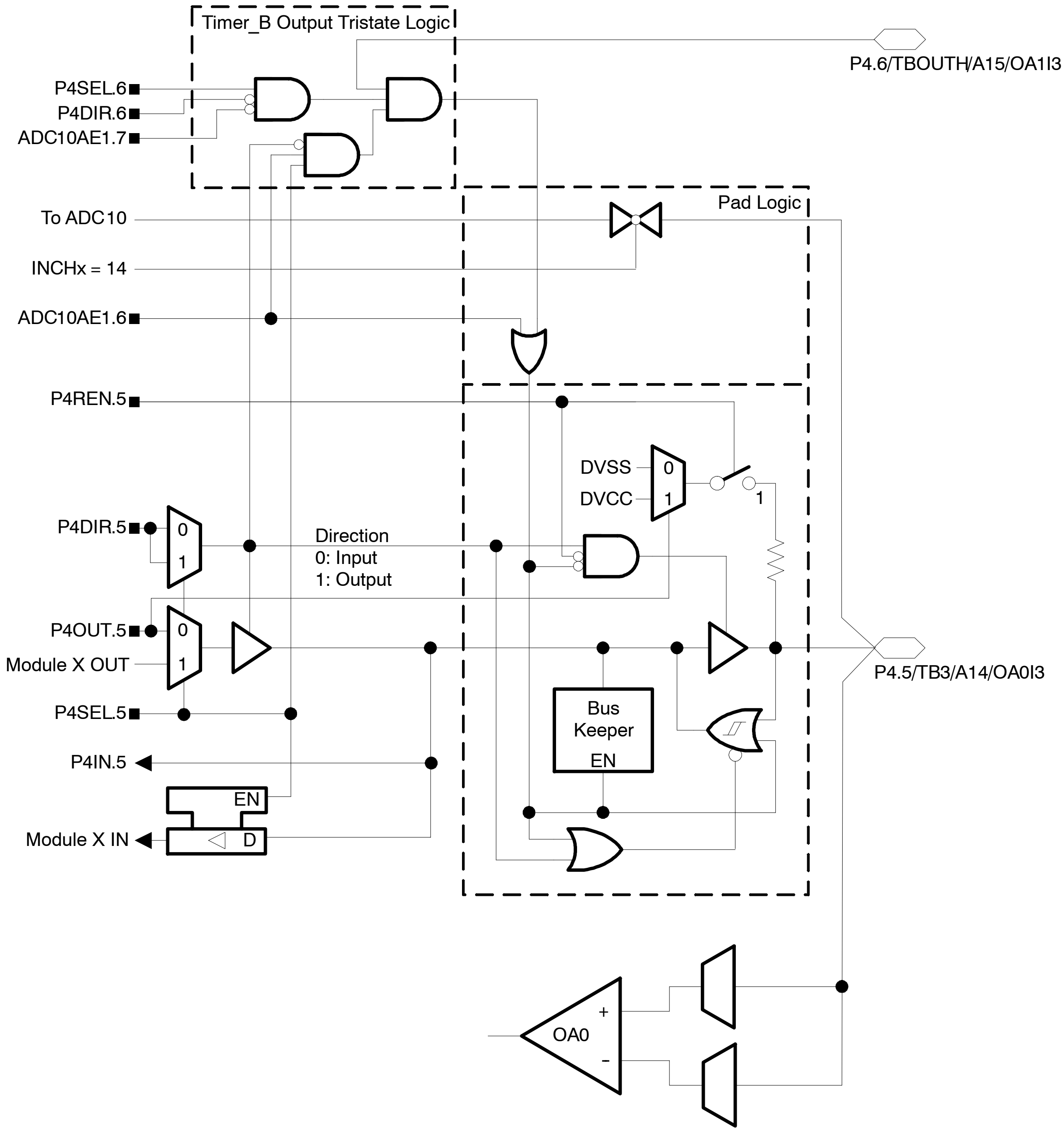
Port P4 (P4.3 to P4.4) pin functions

PIN NAME (P4.X)	X	Y	FUNCTION	CONTROL BITS / SIGNALS		
				P4DIR.x	P4SEL.x	ADC10AE1.y
P4.3/TB0/A12/OA0O	3	4	P4.3† (I/O)	I: 0; O: 1	0	0
			Timer_B3.CCI0B	0	1	0
			Timer_B3.TB0	1	1	0
			A12/OA0O (see Note 3)	X	X	1
P4.4/TB1/A13/OA1O	4	5	P4.4† (I/O)	I: 0; O: 1	0	0
			Timer_B3.CCI1B	0	1	0
			Timer_B3.TB1	1	1	0
			A13/OA1O (see Note 3)	X	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable
2. X: Don’t care
3. Setting the ADC10AE1.y bit disables the output driver as well as the input schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P4 pin schematic: P4.5, input/output with Schmitt trigger



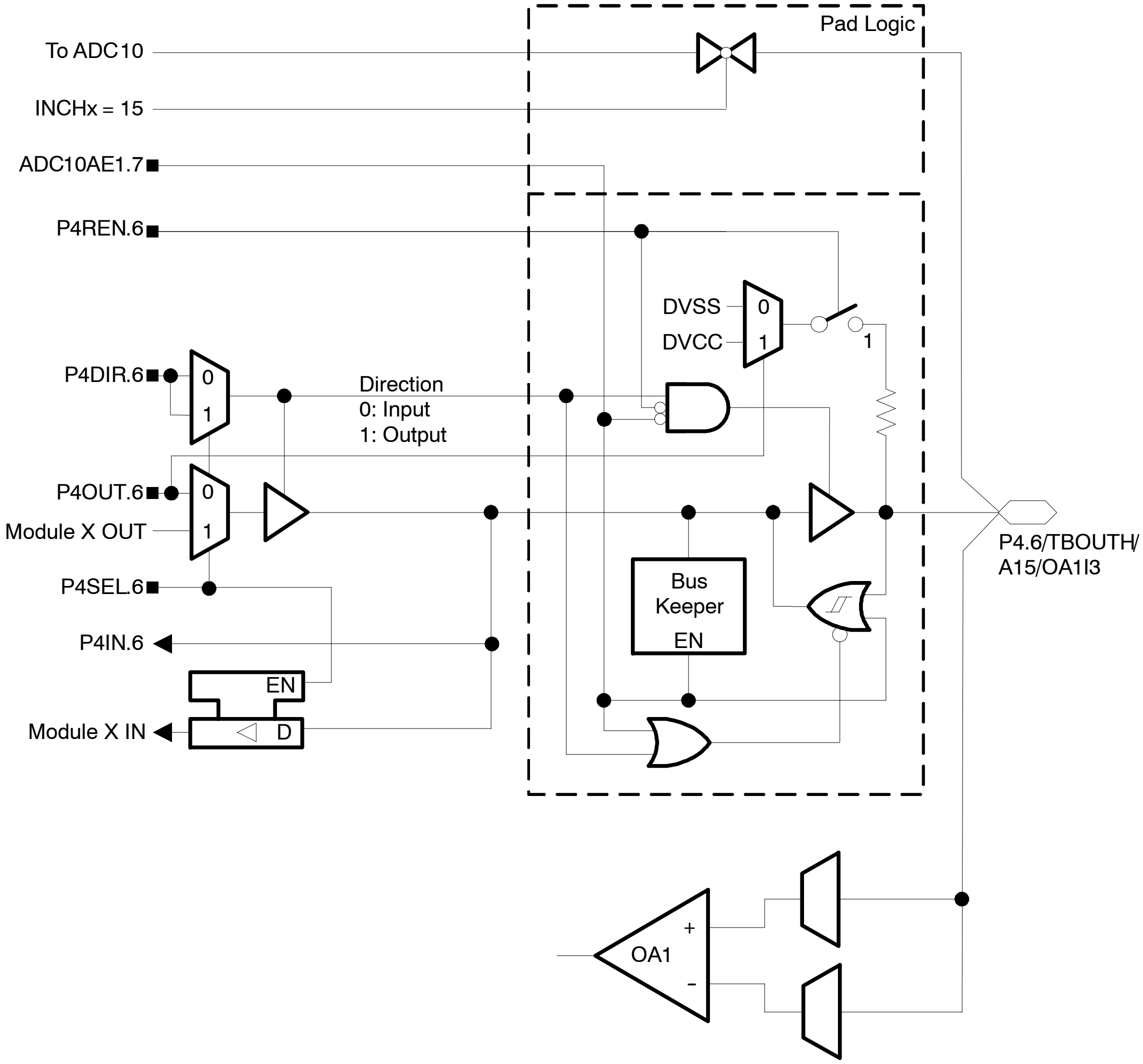
Port P4 (P4.5) pin functions

PIN NAME (P4.X)	X	Y	FUNCTION	CONTROL BITS / SIGNALS		
				P4DIR.x	P4SEL.x	ADC10AE1.y
P4.5/TB3/A14/OA0I3	5	6	P4.5† (I/O)	I: 0; O: 1	0	0
			Timer_B3.TB2	1	1	0
			A14/OA0I3 (see Note 3)	X	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable
2. X: Don't care
3. Setting the ADC10AE1.y bit disables the output driver as well as the input schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P4 pin schematic: P4.6, input/output with Schmitt trigger



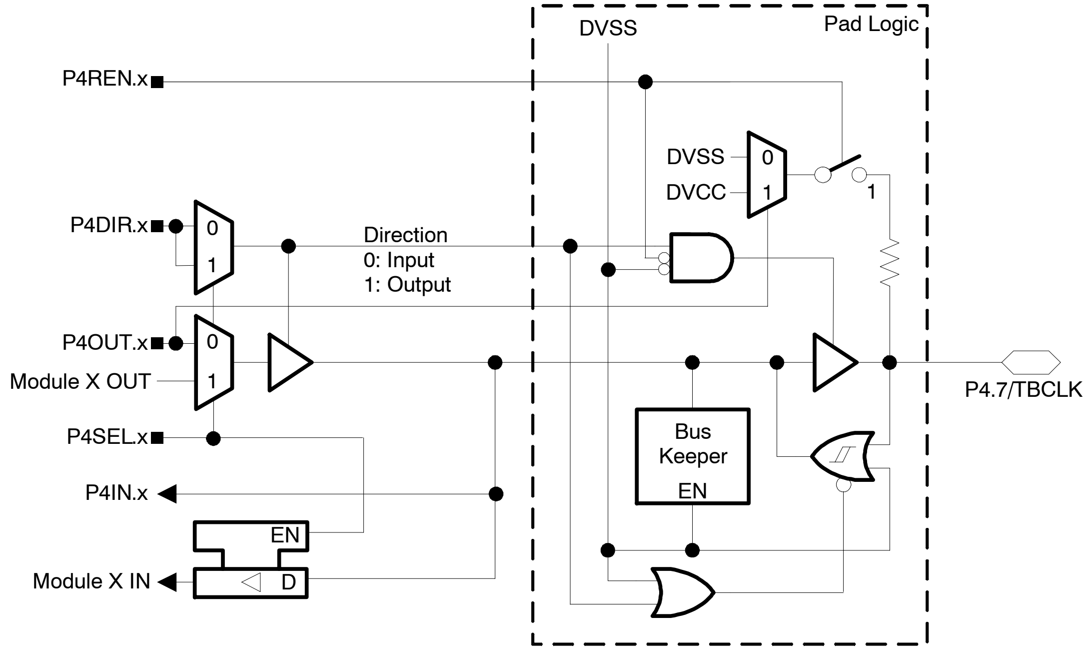
Port P4 (P4.6) pin functions

PIN NAME (P4.X)	X	Y	FUNCTION	CONTROL BITS / SIGNALS		
				P4DIR.x	P4SEL.x	ADC10AE1.y
P4.6/TBOUTH/ A15/OA1I3	6	7	P4.6† (I/O)	I: 0; O: 1	0	0
			TBOUTH	0	1	0
			DV_{SS}	1	1	0
			A15/OA1I3 (see Note 3)	X	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable
2. X: Don't care
3. Setting the ADC10AE1.y bit disables the output driver as well as the input schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P4 pin schematic: P4.7, input/output with Schmitt trigger



Port P4 (P4.7) pin functions

PIN NAME (P4.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P4DIR.x	P4SEL.x
P4.7/TBCLK	7	P4.7† (I/O)	I: 0; O: 1	0
		Timer_B3.TBCLK	0	1
		DV_{SS}	1	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable
2. X: Don't care

JTAG fuse check mode

MSP430 devices that have the fuse on the TEST terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF}, of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TEST pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

When the TEST pin is again taken low after a test or programming session, the fuse check mode and sense currents are terminated.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current only flows when the fuse check mode is active and the TMS pin is in a low state (see Figure 28). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

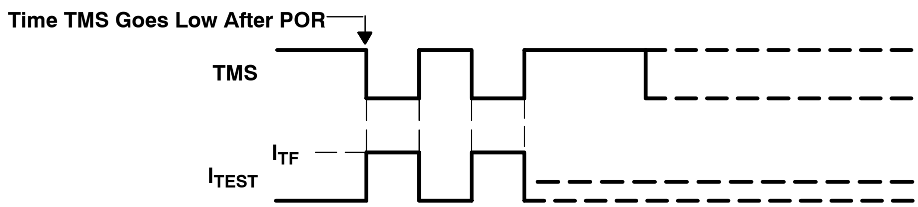


Figure 28. Fuse Check Mode Current, MSP430F22xx

NOTE:

The CODE and RAM data protection is ensured if the JTAG fuse is blown and the 256-bit bootloader access key is used. Also, see the *bootstrap loader* section for more information.

Data Sheet Revision History

Literature Number	Summary
SLAS504	Preliminary data sheet release
SLAS504A	Production data sheet release Updated specification and added characterization graphs Updated/corrected port pin schematics
SLAS504B	Maximum low-power mode supply current limits decreased Added note concerning f_{UCxCLK} to USCI SPI parameters
SLAS504C	Changed T_{stg} for programmed devices from “–40°C to 105°C” to “–55°C to 105°C” (page 23) Added Development Tool Support section (page 2)

NOTE: Page and figure numbers apply to the specific document revision and may differ in other revisions.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
MSP430F2232IDA	ACTIVE	TSSOP	DA	38	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2232IDAR	ACTIVE	TSSOP	DA	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2232IRHAR	ACTIVE	QFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2232IRHAT	ACTIVE	QFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2232TDA	ACTIVE	TSSOP	DA	38	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2232TDAR	ACTIVE	TSSOP	DA	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2232TRHAR	ACTIVE	QFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2232TRHAT	ACTIVE	QFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2234IDA	ACTIVE	TSSOP	DA	38	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2234IDAR	ACTIVE	TSSOP	DA	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2234IRHAR	ACTIVE	QFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2234IRHAT	ACTIVE	QFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2234TDA	ACTIVE	TSSOP	DA	38	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2234TDAR	ACTIVE	TSSOP	DA	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2234TRHAR	ACTIVE	QFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2234TRHAT	ACTIVE	QFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2252IDA	ACTIVE	TSSOP	DA	38	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2252IDAR	ACTIVE	TSSOP	DA	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2252IRHAR	ACTIVE	QFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2252IRHAT	ACTIVE	QFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2252TDA	ACTIVE	TSSOP	DA	38	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2252TDAR	ACTIVE	TSSOP	DA	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2252TRHAR	ACTIVE	QFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2252TRHAT	ACTIVE	QFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2254IDA	ACTIVE	TSSOP	DA	38	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
MSP430F2254IDAR	ACTIVE	TSSOP	DA	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2254IRHAR	ACTIVE	QFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2254IRHAT	ACTIVE	QFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2254TDA	ACTIVE	TSSOP	DA	38	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2254TDAR	ACTIVE	TSSOP	DA	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2254TRHAR	ACTIVE	QFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2254TRHAT	ACTIVE	QFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2272IDA	ACTIVE	TSSOP	DA	38	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2272IDAR	ACTIVE	TSSOP	DA	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2272IRHAR	ACTIVE	QFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2272IRHAT	ACTIVE	QFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2272TDA	ACTIVE	TSSOP	DA	38	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2272TDAR	ACTIVE	TSSOP	DA	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2272TRHAR	ACTIVE	QFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2272TRHAT	ACTIVE	QFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2274IDA	ACTIVE	TSSOP	DA	38	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2274IDAR	ACTIVE	TSSOP	DA	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2274IRHAR	ACTIVE	QFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2274IRHAT	ACTIVE	QFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2274TDA	ACTIVE	TSSOP	DA	38	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2274TDAR	ACTIVE	TSSOP	DA	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
MSP430F2274TRHAR	ACTIVE	QFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2274TRHAT	ACTIVE	QFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF MSP430F2274 :

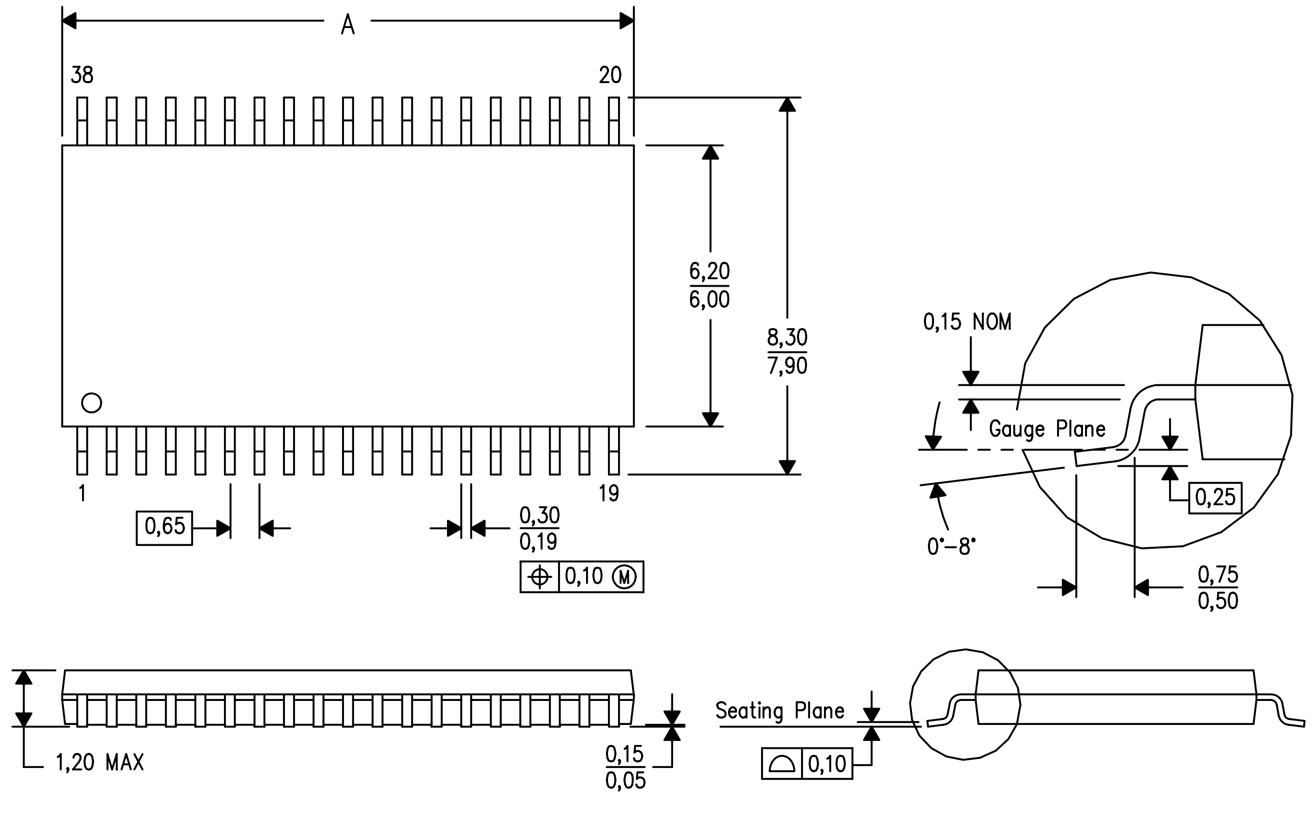
- Enhanced Product: MSP430F2274-EP

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

DA (R–PDSO–G**)   PLASTIC SMALL–OUTLINE PACKAGE

38 PIN SHOWN

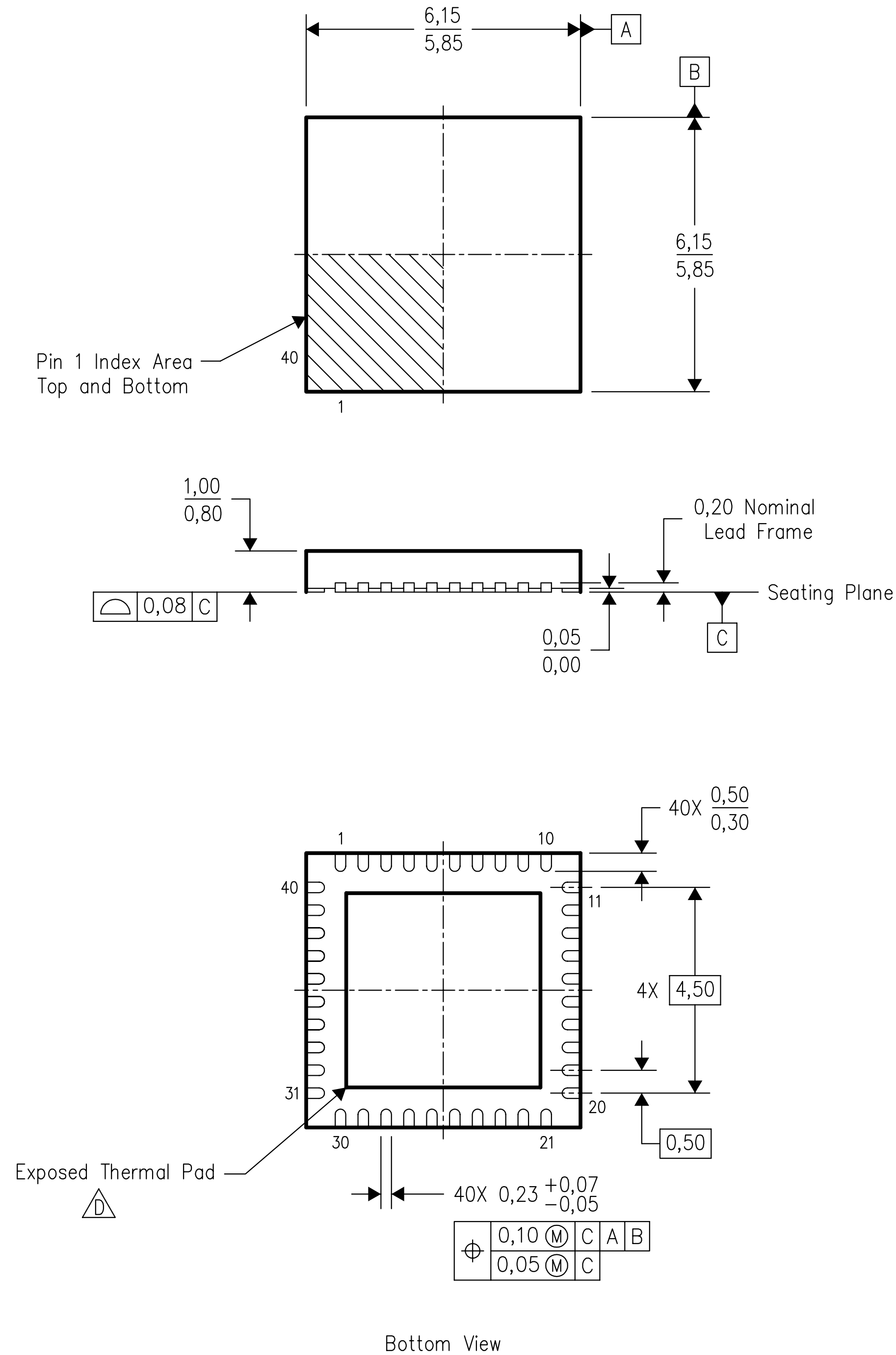


PINS ** / DIM	30	32	38
A MAX	11,10	11,10	12,60
A MIN	10,90	10,90	12,40
D MO–153 Variation	DB–1	DC	DD–1

4040066/F 01/2009

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO–153, except 30 pin body length.

RHA (S-PQFP-N40) PLASTIC QUAD FLATPACK



4204276/C 12/2004

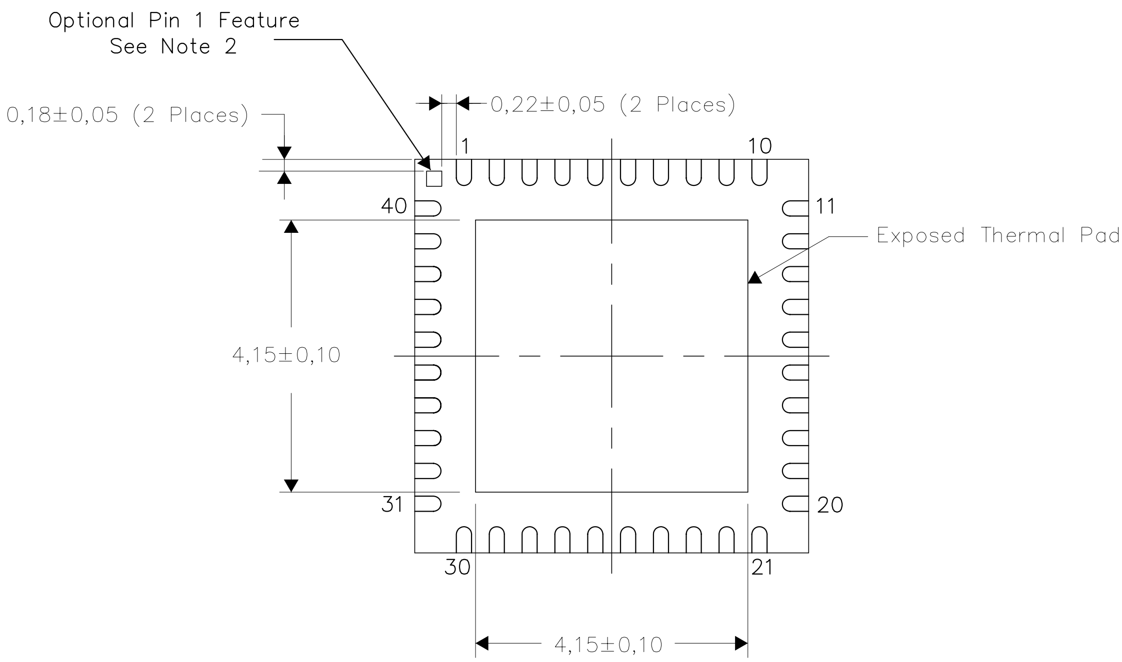
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No−Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO−220 variation VJJD−2.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

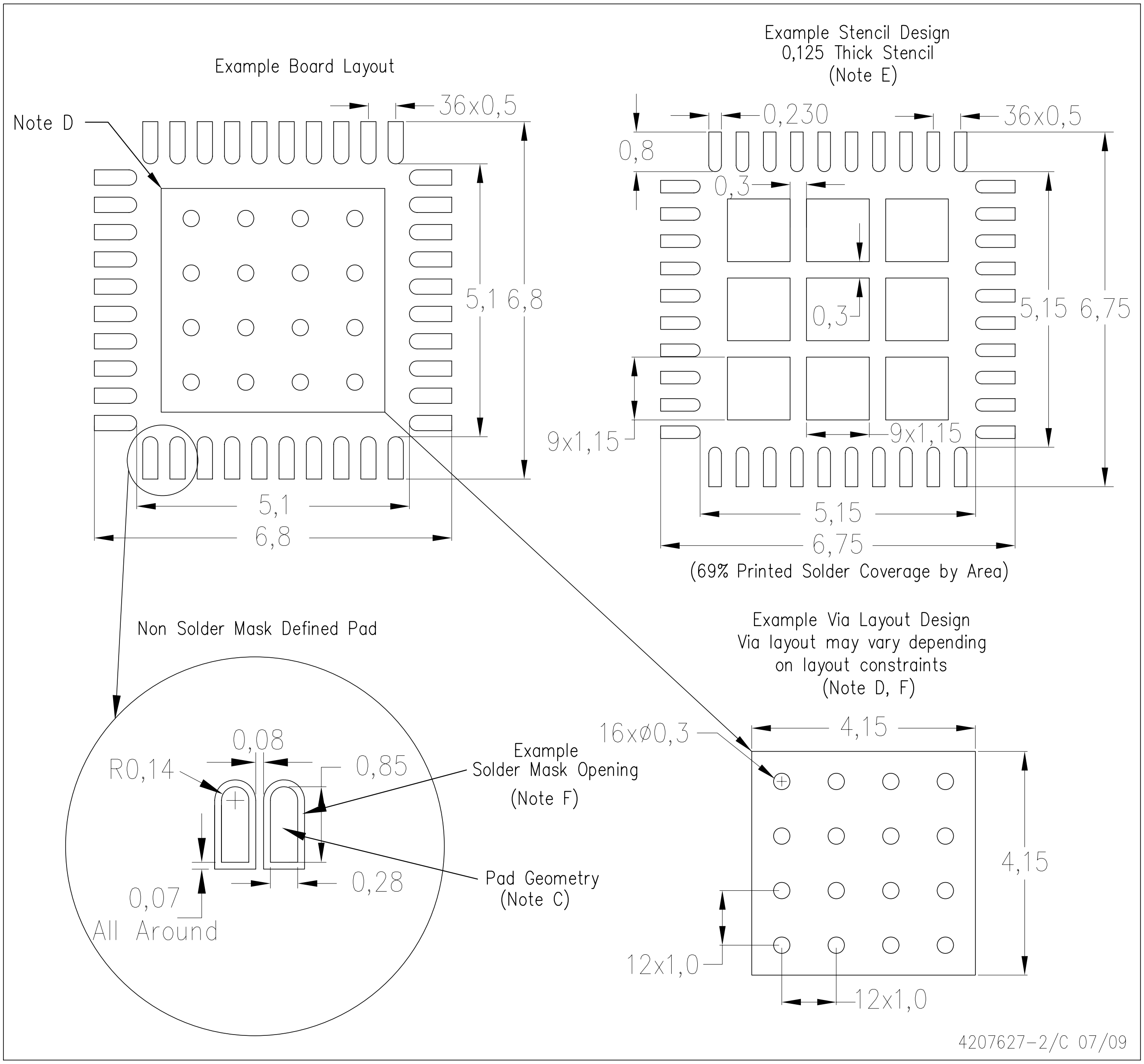


Bottom View

NOTES:
1) All linear dimensions are in millimeters
2) The Pin 1 Identification mark is an optional feature that may be present on some devices In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

Exposed Thermal Pad Dimensions

RHA (S-PVQFN-N40)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.