



Complete 10-Bit, 18-40 MSPS, 50 mW CMOS A/D Converter

Preliminary Technical Information

AD9203

FEATURES

CMOS 10-Bit 18-40 MSPS Sampling A/D Converter
Pin-Compatible with AD9202
Power Dissipation: 50 mW (3V Supply, 40 MSPS)
Operation Between 2.7 V and 3.6 V Supply
Differential Nonlinearity: 0.5 LSB
Power-Down (Sleep) Mode
ENOB: 8.5 @ 40 MSPS
9 @ 18 MSPS
Out-of-Range Indicator
Adjustable On-Chip Voltage Reference
IF Undersampling to 135 MHz
Input range: 2V pp differential or single ended low power
Adjustable Power Consumption

PRODUCT DESCRIPTION

The AD9203 is a monolithic low power, single supply, 10-bit, 18-40 MSPS analog-to-digital converter with an on-chip sample-and-hold amplifier and voltage reference. The AD9203 uses a multistage differential pipeline architecture at 40 MSPS data rates and guarantees no missing codes over the full operating temperature range.

The AD9203 is characterized at 18 MSPS and 40 MSPS for use in a wide range of imaging and communications systems.

The AD9203 has an onboard programmable reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application.

An external resistor can be used to scale the power consumption when operating at lower sampling rates.

A single clock input is used to control all internal conversion cycles. The digital output data is presented in straight binary output format. An out-of-range signal (OTR) indicates an over-flow condition which can be used with the most significant bit to determine low or high overflow.

The AD9203 can operate with supply range from 2.7 V to 3.6 V, ideally suiting it for low power operation in high speed portable applications.

The AD9203 is specified over the industrial (-40°C to +85°C) temperature ranges.

PRODUCT HIGHLIGHTS

Low Power

The AD9203 consumes 50 mW on a 3 V supply operating at 40 MSPS. In sleep mode, power is reduced to below 3 mW.

Very Small Package

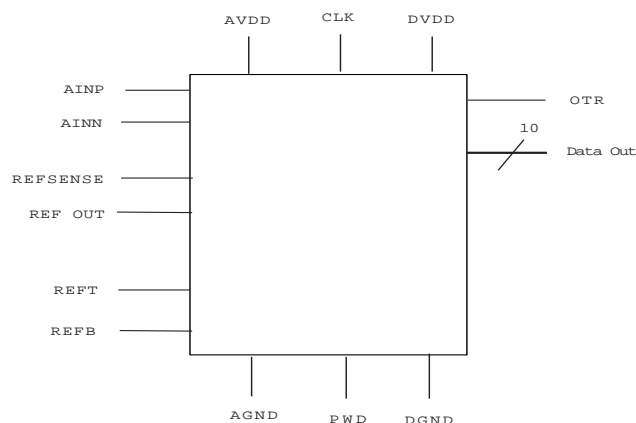
The AD9203 is available in a 28-pin TSSOP and SSOP.

Pin compatible with AD9202

The AD9203 is pin compatible with the AD9202.

Out-of-Range Indicator

The OTR output bit indicates when the input signal is beyond the AD9203's input range.



AD9203 - SPECIFICATIONS

(AVDD= +3V, DRVDD = +3 V, FS = 32 MHz 50% Duty Cycle, MODE = AVDD, 2 V Input Span from 0.5 V to 2.5V, External Reference, TMIN to TMAX unless otherwisw noted)

Parameter	Symbol	Min	Typ	Max	Units	Conditions
RESOLUTION			10		Bits	
CONVERSION RATE	F_s			40	MHz	
DC ACCURACY						
Differential Nonlinearity	DNL		±0.5	±1	LSB	
Integral Nonlinearity	INL		±0.75	±2	LSB	
Offset Error	EZS		0.4	1.2	% FSR	
Gain Error	EFS		1.4	3.5	% FSR	
ANALOG INPUT						
Input Voltage Range	AIN			2	V	Differential or single ended
Input Capacitance	CIN		1.5		pF	Switched
Aperture Delay	tAP		4		ns	
Aperture Uncertainty (Jitter)	tAJ		2		ps	
Input Bandwidth (-3dB)	BW					
Full Power (0 dB)			300		MHz	
INTERNAL REFERENCE						
Output Voltage (0.5 V Mode)	VREF		0.5		V	REFSENSE = VREF
Output Voltage Tolerance (1 V Mode)			±5	±10	mV	
Output Voltage (1 V Mode)	VREF		1		V	REFSENSE = GND
POWER SUPPLY						
Operating Voltage	AVDD	2.7	3	3.6	V	
	DRVDD	2.7	3	3.6	V	
Supply Current	IAVDD		TBD	TBD	mA	AVDD=3 V,
Power Consumption						
@40 MSPS	PD		50	TBD	mW	AVDD=DRVDD=3 V,
@18 MSPS			25			
Power-down			3		mW	STBY = AVDD,
Gain Error Power	PSRR		TBD		%FS	
Supply Rejection						

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Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units	Condition
At FS=			18			40		MSPS	
DYNAMIC PERFORMANCE (AIN=0.5 dBFS)									
Signal-to-Noise and Distortion	SINAD								* differential input
f=3.58 MHz			55			TBD		dB	
f=10 MHz			TBD			TBD		dB	
Effective Bits									
f=3.58 MHz			9			8.5		Bits	* differential input
f=10 MHz			TBD			TBD		Bits	
Signal-to-Noise	SNR								
f=3.58 MHz			57			TBD		dB	
f=10 MHz			TBD			TBD		dB	
Total Harmonic Distortion	TBD								
f=3.58 MHz			60			TBD		dB	* differential input
f=10 MHz			TBD			TBD		dB	
Spurious Free Dynamic Range	SFDR								
f=3.58 MHz			62			TBD		dB	* differential input
f=10 MHz						TBD		dB	
Two-Tone Intermodulation Distortion	IMD		TBD			TBD		dB	* differential input f=44.49 MHz & 45.52 MHz
Differential Phase	DP		0.2			0.2		Degree	NTSC 40 IRE Mode Ramp
Differential Gain	DG		1			1		%	

* with single ended input typical values degrade slightly (TBD)

