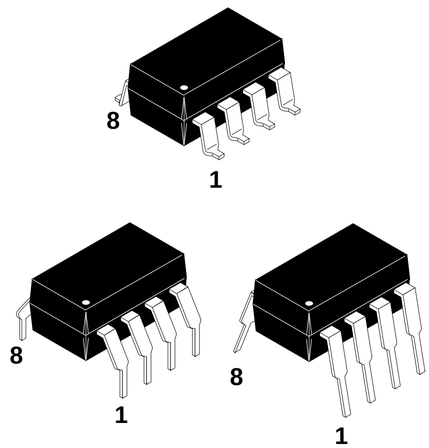
HIGH SPEED-10 MBit/s LOGIC GATE OPTOCOUPLERS

FAIRCHILD SEMICONDUCTOR™

SINGLE-CHANNEL	DUAL-CHANNEL
6N137	HCPL-2630
HCPL-2601	HCPL-2631
HCPL-2611	



DESCRIPTION

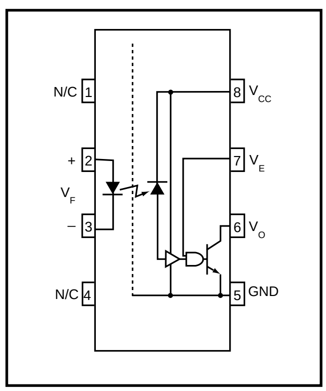
The 6N137, HCPL-2601/2611 single-channel and HCPL-2630/2631 dual-channel optocouplers consist of a 850 nm AlGaAS LED, optically coupled to a very high speed integrated photodetector logic gate with a strobable output. This output features an open collector, thereby permitting wired OR outputs. The coupled parameters are guaranteed over the temperature range of -40°C to +85°C. A maximum input signal of 5 mA will provide a minimum output sink current of 13 mA (fan out of 8).

An internal noise shield provides superior common mode rejection of typically 10 kV/µs. The HCPL- 2601 and HCPL- 2631 has a minimum CMR of 5 kV/µs.

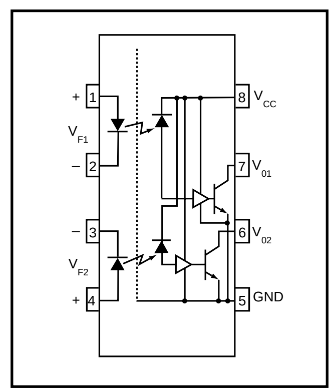
The HCPL-2611 has a minimum CMR of 10 kV/µs.

FEATURES

- Very high speed-10 MBit/s
- Superior CMR-10 kV/µs
- Double working voltage-480V
- Fan-out of 8 over -40°C to +85°C
- Logic gate output
- Strobable output
- Wired OR-open collector
- U.L. recognized (File # E90700)



Single-channel circuit drawing



Dual-channel circuit drawing

APPLICATIONS

- Ground loop elimination
- LSTTL to TTL, LSTTL or 5-volt CMOS
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer-peripheral interface

TRUTH TABLE
(Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H
H	NC	L
L	NC	H

A 0.1 µF bypass capacitor must be connected between pins 8 and 5.
(See note 1)

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ABSOLUTE MAXIMUM RATINGS (No derating required up to 85°C)

Parameter		Symbol	Value	Units
Storage Temperature		T_{STG}	-55 to +125	°C
Operating Temperature		T_{OPR}	-40 to +85	°C
Lead Solder Temperature		T_{SOL}	260 for 10 sec	°C
EMITTER				
DC/Average Forward Input Current	Single channel	I_F	50	mA
	Dual channel (Each channel)		30	
Enable Input Voltage Not to exceed V_{CC} by more than 500 mV	Single channel	V_E	5.5	V
Reverse Input Voltage	Each channel	V_R	5.0	V
Power Dissipation	Single channel	P_I	100	mW
	Dual channel (Each channel)		45	
DETECTOR				
Supply Voltage		V_{CC} (1 minute max)	7.0	V
Output Current	Single channel	I_O	50	mA
	Dual channel (Each channel)		50	
Output Voltage	Each channel	V_O	7.0	V
Collector Output Power Dissipation	Single channel	P_O	85	mW
	Dual channel (Each channel)		60	

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Units
Input Current, Low Level	I_{FL}	0	250	µA
Input Current, High Level	I_{FH}	*6.3	15	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Enable Voltage, Low Level	V_{EL}	0	0.8	V
Enable Voltage, High Level	V_{EH}	2.0	V_{CC}	V
Low Level Supply Current	T_A	-40	+85	°C
Fan Out (TTL load)	N		8	

* 6.3 mA is a guard banded value which allows for at least 20 % CTR degradation. Initial input current threshold value is 5.0 mA or less

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ELECTRICAL CHARACTERISTICS (T_A = -40°C to +85°C Unless otherwise specified.)

INDIVIDUAL COMPONENT CHARACTERISTICS

Parameter		Test Conditions	Symbol	Min	Typ**	Max	Unit
EMITTER Input Forward Voltage		(I_F = 10 mA)	V_F			1.8	V
		T_A =25°C			1.4	1.75	
Input Reverse Breakdown Voltage		(I_R = 10 µA)	B_{VR}	5.0			V
Input Capacitance		(V_F = 0, f = 1 MHz)	C_{IN}		60		pF
Input Diode Temperature Coefficient		(I_F = 10 mA)	$\Delta V_F/\Delta T_A$		-1.4		mV/°C
DETECTOR High Level Supply Current	Single Channel	(V_{CC} = 5.5 V, I_F = 0 mA)	I_{CCH}		7	10	mA
	Dual Channel	(V_E = 0.5 V)			15	20	
Low Level Supply Current	Single Channel	(V_{CC} = 5.5 V, I_F = 10 mA)	I_{CCL}		9	13	mA
	Dual Channel	(V_E = 0.5 V)			19	26	
Low Level Enable Current		(V_{CC} = 5.5 V, V_E = 0.5 V)	I_{EL}		-0.8	-1.6	mA
High Level Enable Current		(V_{CC} = 5.5 V, V_E = 2.0 V)	I_{EH}		-0.6	-1.6	mA
High Level Enable Voltage		(V_{CC} = 5.5 V, I_F = 10 mA)	V_{EH}	2.0			V
Low Level Enable Voltage		(V_{CC} = 5.5 V, I_F = 10 mA) (Note 3)	V_{EL}			0.8	V

SWITCHING CHARACTERISTICS (T_A = -40°C to +85°C, V_{CC} = 5 V, I_F = 7.5 mA Unless otherwise specified.)

AC Characteristics		Test Conditions	Symbol	Min	Typ**	Max	Unit
Propagation Delay Time to Output High Level		(Note 4) (T_A =25°C)	T_{PLH}	20	45	75	ns
		(R_L = 350 Ω, C_L = 15 pF) (Fig. 12)				100	
Propagation Delay Time to Output Low Level		(Note 5) (T_A =25°C)	T_{PHL}	25	45	75	ns
		(R_L = 350 Ω, C_L = 15 pF) (Fig. 12)				100	
Pulse Width Distortion		(R_L = 350 Ω, C_L = 15 pF) (Fig. 12)	$\|T_{PHL}-T_{PLH}\|$		3	35	ns
Output Rise Time (10-90%)		(R_L = 350 Ω, C_L = 15 pF) (Note 6) (Fig. 12)	t_r		50		ns
Output Fall Time (90-10%)		(R_L = 350 Ω, C_L = 15 pF) (Note 7) (Fig. 12)	t_f		12		ns
Enable Propagation Delay Time to Output High Level		(I_F = 7.5 mA, V_{EH} = 3.5 V) (R_L = 350 Ω, C_L = 15 pF) (Note 8) (Fig. 13)	t_{ELH}		20		ns
Enable Propagation Delay Time to Output Low Level		(I_F = 7.5 mA, V_{EH} = 3.5 V) (R_L = 350 Ω, C_L = 15 pF) (Note 9) (Fig. 13)	t_{EHL}		20		ns
Common Mode Transient Immunity (at Output High Level)		(T_A =25°C) $\|V_{CM}\|$ = 50 V, (Peak) (I_F = 0 mA, V_{OH} (Min.) = 2.0 V)	$\|CM_H\|$				V/µs
	6N137, HCPL-2630	(R_L = 350 Ω) (Note 10)			10,000		
	HCPL-2601, HCPL-2631	(Fig. 14)		5000	10,000		
	HCPL-2611	$\|V_{CM}\|$ = 400 V		10,000	15,000		
Common Mode Transient Immunity (at Output Low Level)		(R_L = 350 Ω) (I_F = 7.5 mA, V_{OL} (Max.) = 0.8 V)	$\|CM_L\|$				V/µs
	6N137, HCPL-2630	$\|V_{CM}\|$ = 50 V (Peak)			10,000		
	HCPL-2601, HCPL-2631	(T_A =25°C) (Note 11) (Fig. 14)		5000	10,000		
	HCPL-2611 (T_A =25°C)	$\|V_{CM}\|$ = 400 V		10,000	15,000		

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TRANSFER CHARACTERISTICS (T_A = -40°C to +85°C Unless otherwise specified.)

DC Characteristics	Test Conditions	Symbol	Min	Typ**	Max	Unit
High Level Output Current	(V_{CC} = 5.5 V, V_O = 5.5 V) (I_F = 250 µA, V_E = 2.0 V) (Note 2)	I_{OH}			100	µA
Low Level Output Current	(V_{CC} = 5.5 V, I_F = 5 mA) (V_E = 2.0 V, I_{CL} = 13 mA) (Note 2)	V_{OL}		.35	.06	V
Input Threshold Current	(V_{CC} = 5.5 V, V_O = 0.6 V, V_E = 2.0 V, I_{OL} = 13 mA)	I_{FT}		3	5	mA

ISOLATION CHARACTERISTICS (T_A = -40°C to +85°C Unless otherwise specified.)

Characteristics	Test Conditions	Symbol	Min	Typ**	Max	Unit
Input-Output Insulation Leakage Current	(Relative humidity = 45%) (T_A = 25°C, t = 5 s) (V_{I-O} = 3000 VDC) (Note 12)	I_{I-O}			1.0*	µA
Withstand Insulation Test Voltage	(RH < 50%, T_A = 25°C) (Note 12) (t = 1 min.)	V_{ISO}	2500			V_{RMS}
Resistance (Input to Output)	(V_{I-O} = 500 V) (Note 12)	R_{I-O}		10^{12}		Ω
Capacitance (Input to Output)	(f = 1 MHz) (Note 12)	C_{I-O}		0.6		pF

** All typical values are at V_{CC} = 5 V, T_A = 25°C

NOTES

1. The V_{CC} supply to each optoisolator must be bypassed by a 0.1µF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and GND pins of each device.
2. Each channel.
3. Enable Input - No pull up resistor required as the device has an internal pull up resistor.
4. t_{PLH} - Propagation delay is measured from the 3.75 mA level on the HIGH to LOW transition of the input current pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.
5. t_{PHL} - Propagation delay is measured from the 3.75 mA level on the LOW to HIGH transition of the input current pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.
6. t_r - Rise time is measured from the 90% to the 10% levels on the LOW to HIGH transition of the output pulse.
7. t_f - Fall time is measured from the 10% to the 90% levels on the HIGH to LOW transition of the output pulse.
8. t_{ELH} - Enable input propagation delay is measured from the 1.5 V level on the HIGH to LOW transition of the input voltage pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.
9. t_{EHL} - Enable input propagation delay is measured from the 1.5 V level on the LOW to HIGH transition of the input voltage pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.
10. CM_H - The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the high state (i.e., V_{OUT} > 2.0 V). Measured in volts per microsecond (V/µs).
11. CM_L - The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the low output state (i.e., V_{OUT} < 0.8 V). Measured in volts per microsecond (V/µs).
12. Device considered a two-terminal device: Pins 1,2,3 and 4 shorted together, and Pins 5,6,7 and 8 shorted together.

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Fig.1 Low Level Output Voltage vs. Ambient Temperature

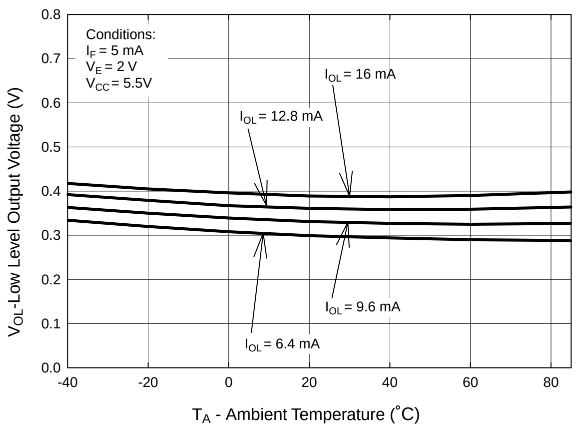

Fig. 2 Input Diode Forward Voltage vs. Forward Current

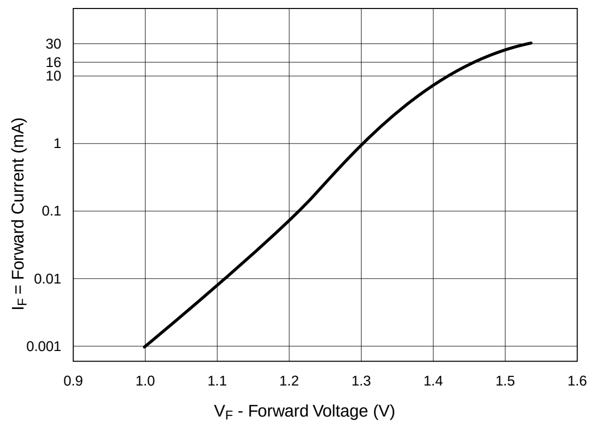

Fig.3 Switching Time vs. Forward Current

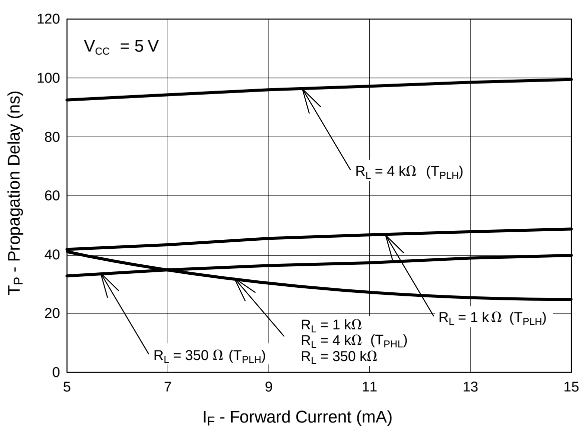

Fig. 4 Low Level Output Current vs. Ambient Temperature

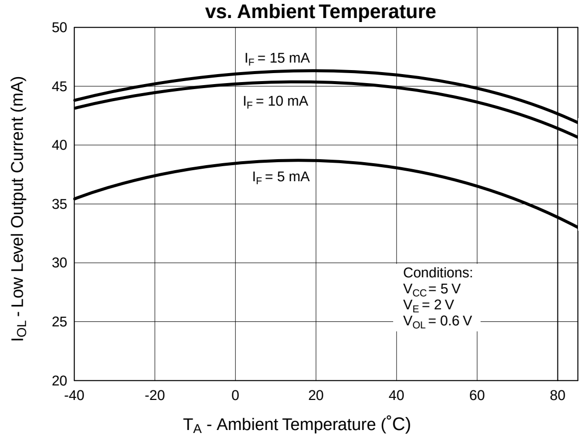

Fig. 5 Input Threshold Current vs. Ambient Temperature

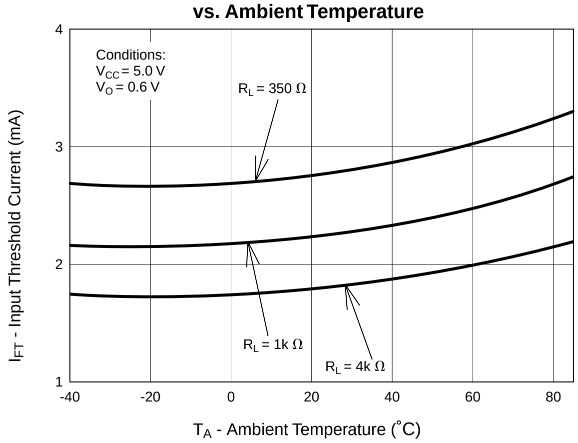

Fig. 6 Output Voltage vs. Input Forward Current

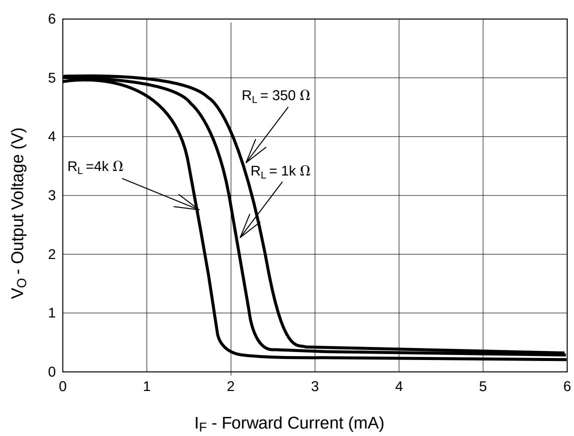

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Fig. 7 Pulse Width Distortion vs. Temperature

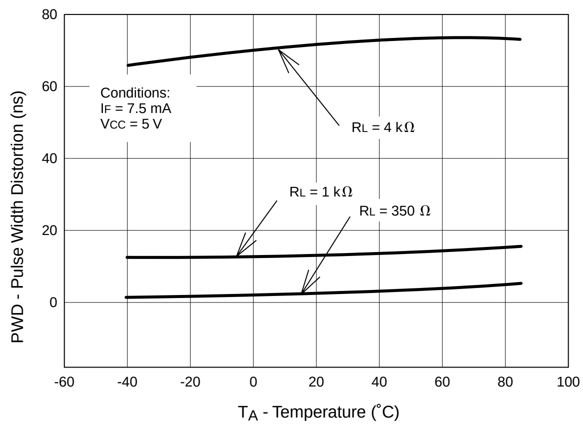


Fig. 8 Rise and Fall Time vs. Temperature

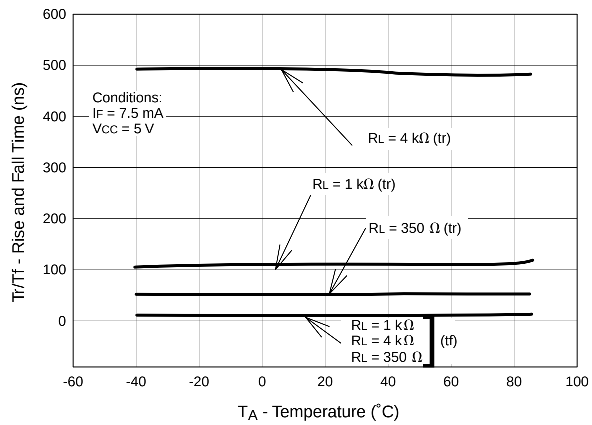


Fig. 9 Enable Propagation Delay vs. Temperature

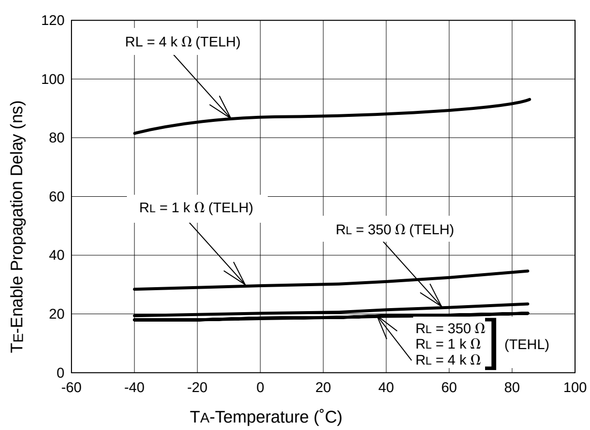


Fig. 10 Switching Time vs. Temperature

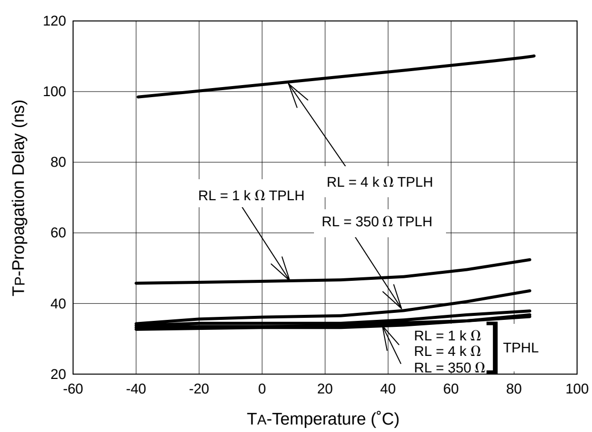
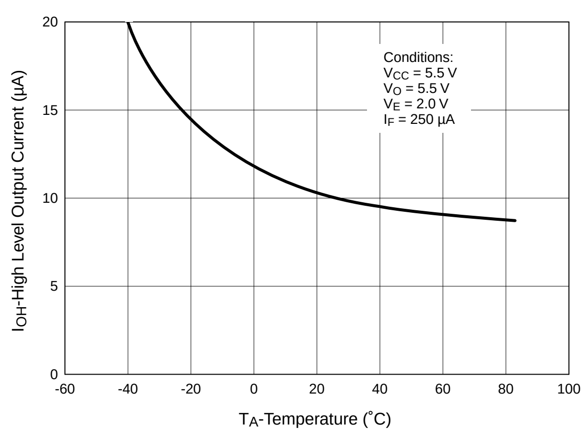


Fig. 11 High Level Output Current vs. Temperature



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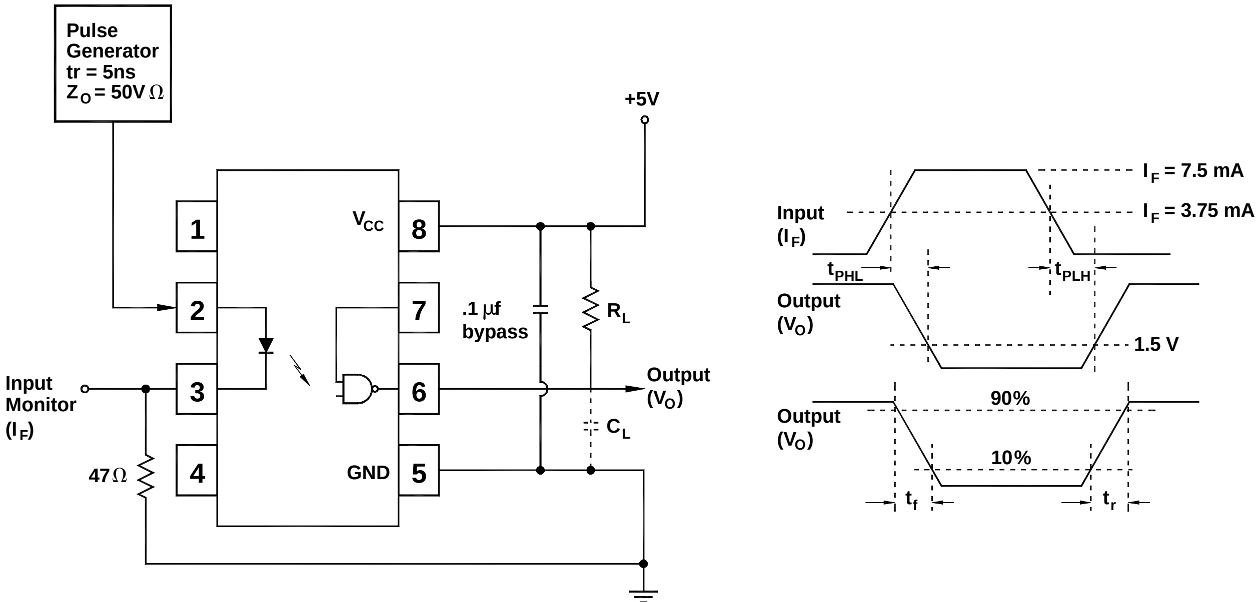

Fig. 12 Test Circuit and Waveforms for t_{PLH}, t_{PHL}, t_r and t_f.

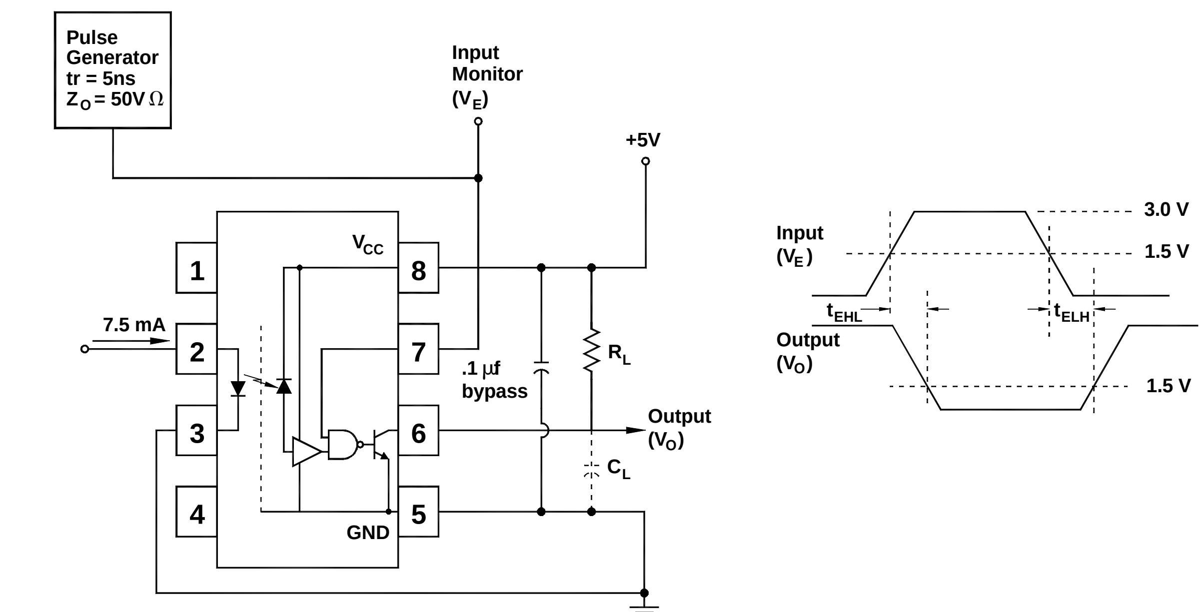

Fig. 13 Test Circuit t_{EHL} and t_{ELH}.

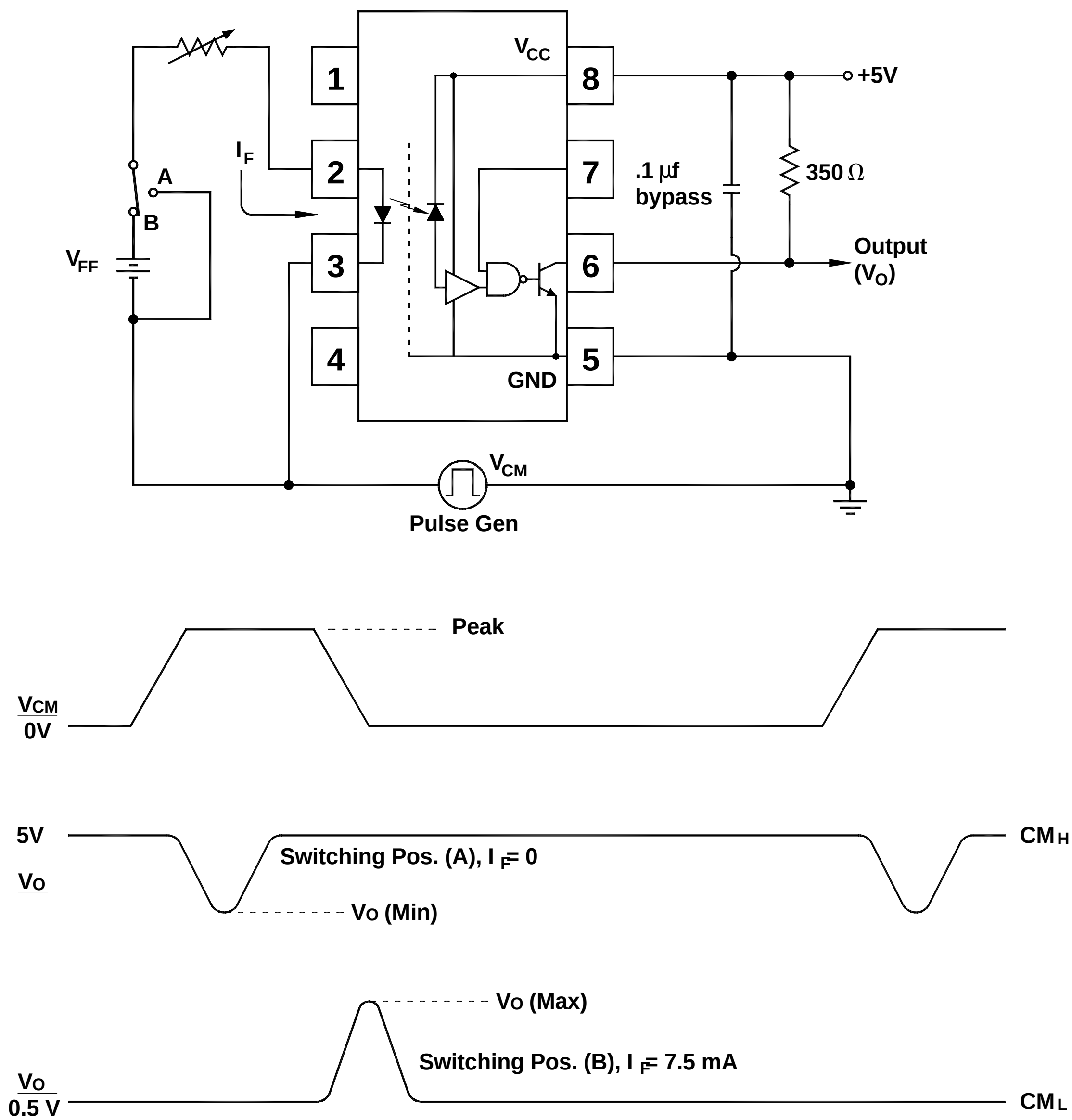

Fig. 14 Test Circuit Common Mode Transient Immunity

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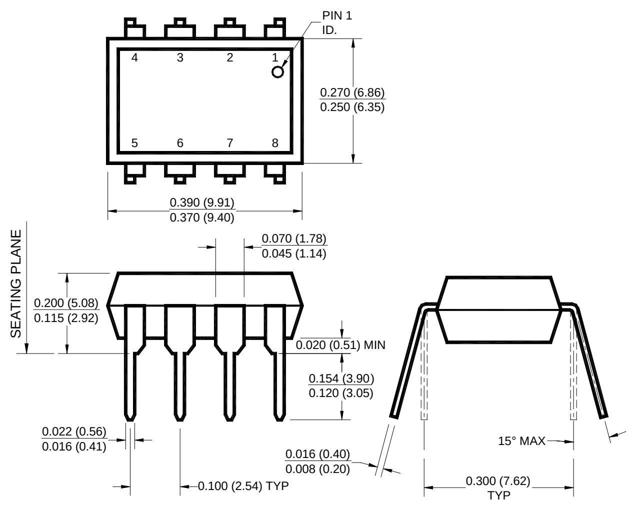
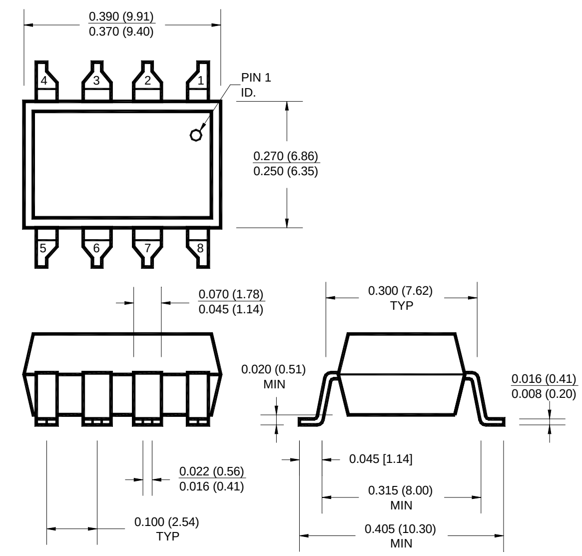
Package Dimensions (Through Hole)

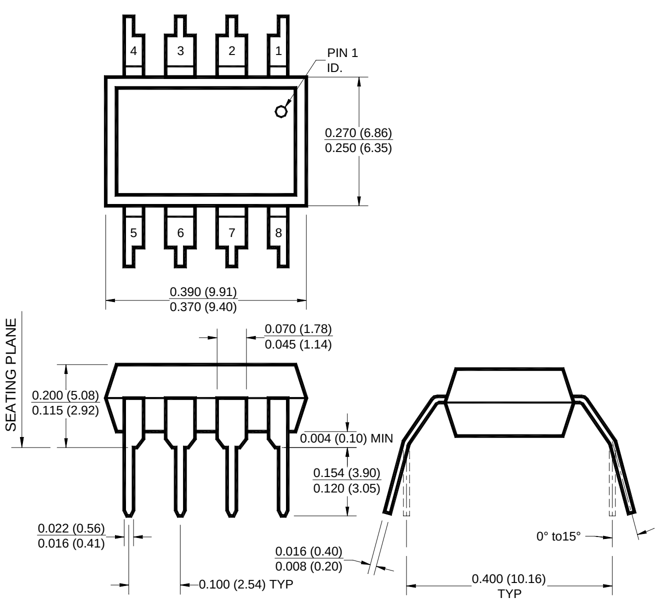


Package Dimensions (Surface Mount)



Lead Coplanarity : 0.004 (0.10) MAX

Package Dimensions (0.4”Lead Spacing)



NOTE

All dimensions are in inches (millimeters)

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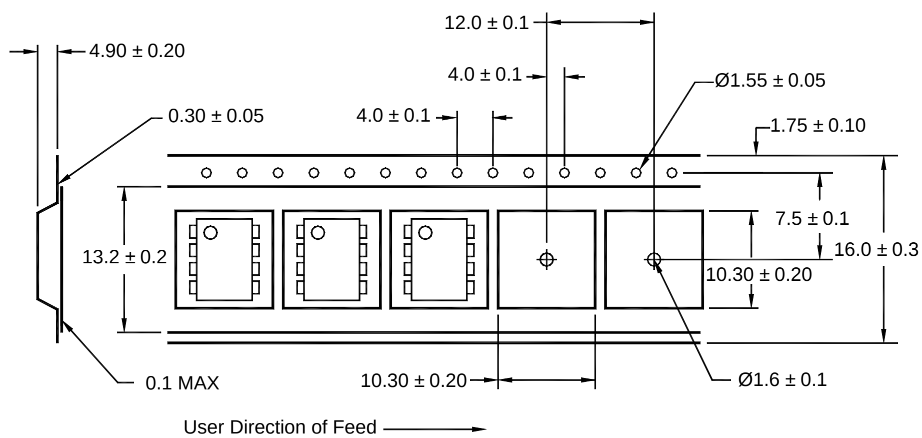
ORDERING INFORMATION

Option	Order Entry Identifier	Description
R2	.R2	Opto Plus Reliability Conditioning
S	.S	Surface Mount Lead Bend
SD	.SD	Surface Mount; Tape and reel
W	.W	0.4" Lead Spacing

QT Carrier Tape Specifications ("D" Taping Orientation)



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