RELIABILITY REPORT

FOR

MAX1771xxA

PLASTIC ENCAPSULATED DEVICES

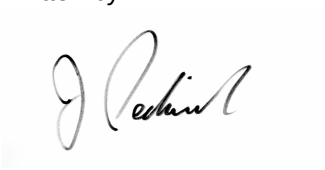
July 28, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



Jim Pedicord
Quality Assurance
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Reviewed by

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Conclusion

The MAX1771 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1771 step-up switching controller provides 90% efficiency over a 30mA to 2A load. A unique current-limited pulse-frequency-modulation (PFM) control scheme gives this device the benefits of pulse-width-modulation (PWM) converters (high efficiency at heavy loads), while using less than 110µA of supply current (vs. 2mA to 10mA for PWM converters).

This controller uses miniature external components. Its high switching frequency (up to 300kHz) allows surface-mount magnetics of 5mm height and 9mm diameter. It accepts input voltages from 2V to 16.5V. The output voltage is preset at 12V, or can be adjusted using two resistors.

The MAX1771 optimizes efficiency at low input voltages and reduces noise by using a single 100mV current-limit threshold under all load conditions. The MAX1771 drives an external N-channel MOSFET switch, allowing it to power loads up to 24W.

B. Absolute Maximum Ratings

Item	Rating
Supply Voltage	
V+ to GND	-0.3V, 17V
EXT, CS, REF, SHDN, FB to GND	-0.3V, (V+ + 0.3V)
GND to AGND	0.1V, -0.1V
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	471mW
Derates above +70°C	5.88mW/°C
Continuous Power Dissipation (TA = 70°C)	
8-Pin SO	471mW
8-Pin PDIP	727mW
Derates above +70°C	
8-Pin SO	5.88mW/°C
8-Pin PDIP	9.09mW/°C

II. Manufacturing Information

A. Description/Function:	12V or Adjustable, High-Efficiency, Low IQ, Step-Up DC-DC Controller
B. Process:	SG5 (Standard 5 micron silicon gate CMOS)
C. Number of Device Transistors:	501
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines, Malaysia, or Thailand
F. Date of Initial Production:	June, 1994

III. Packaging Information

A. Package Type:	**8-Lead NSO**	**8-Lead PDIP**
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1701-0124	# 05-1701-0123
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	80 x 126 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	5 microns (as drawn)
F. Minimum Metal Spacing:	5 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 800 \times 2}$$

1.83 (Chi square value for MTTF upper limit)

192 x 4389 x 800 x 2 — Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 1.36 \times 10^{-9}$ $\lambda = 1.36$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-0091) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PW09-5 die type has been found to have all pins able to withstand a transient pulse of ±2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX1771xxA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		800	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	NSO PDIP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

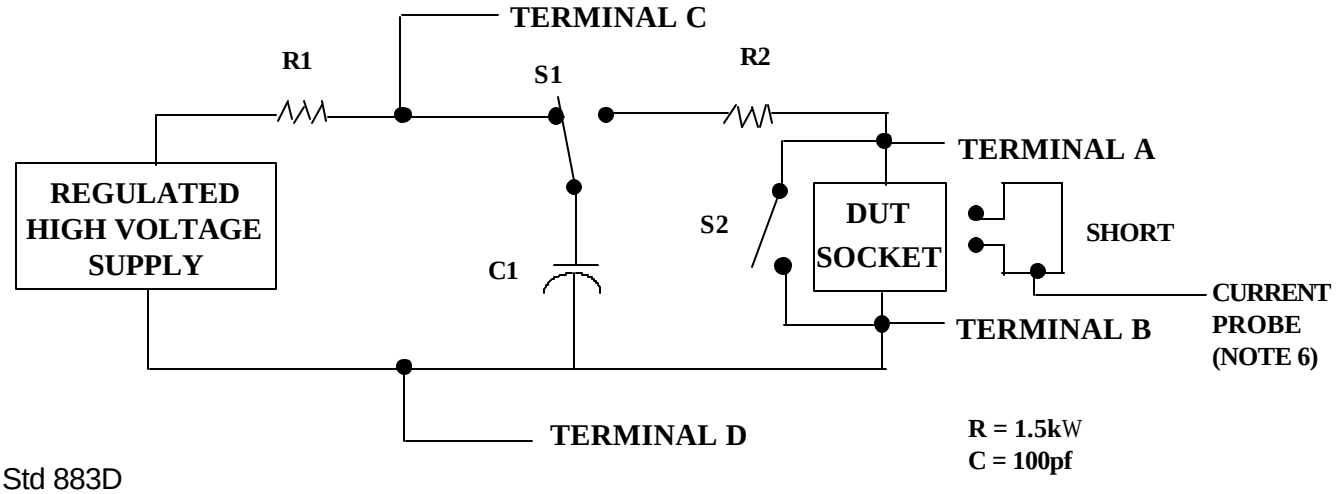
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

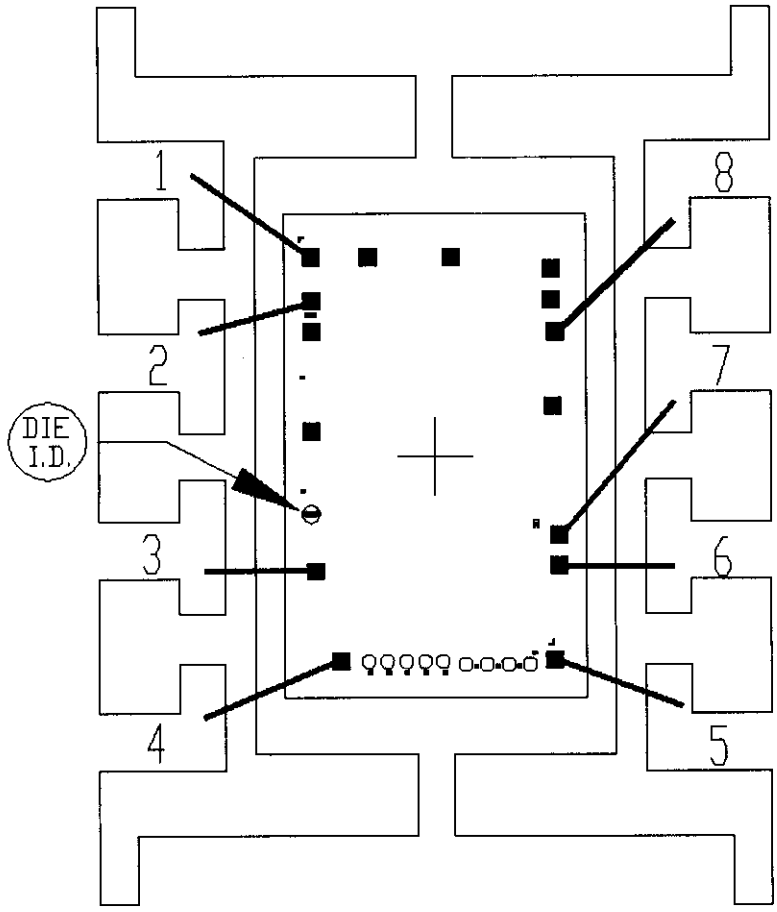
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

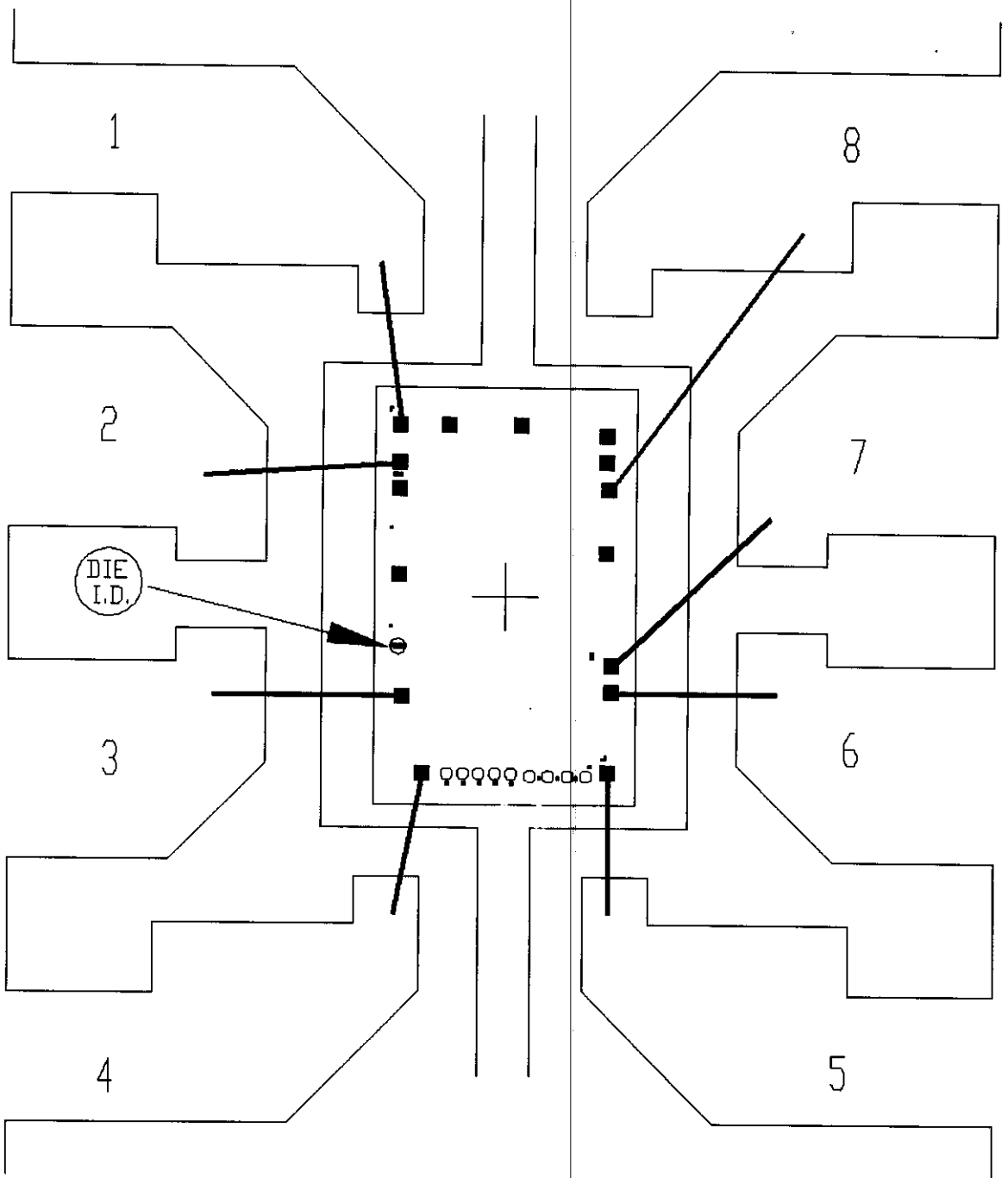
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



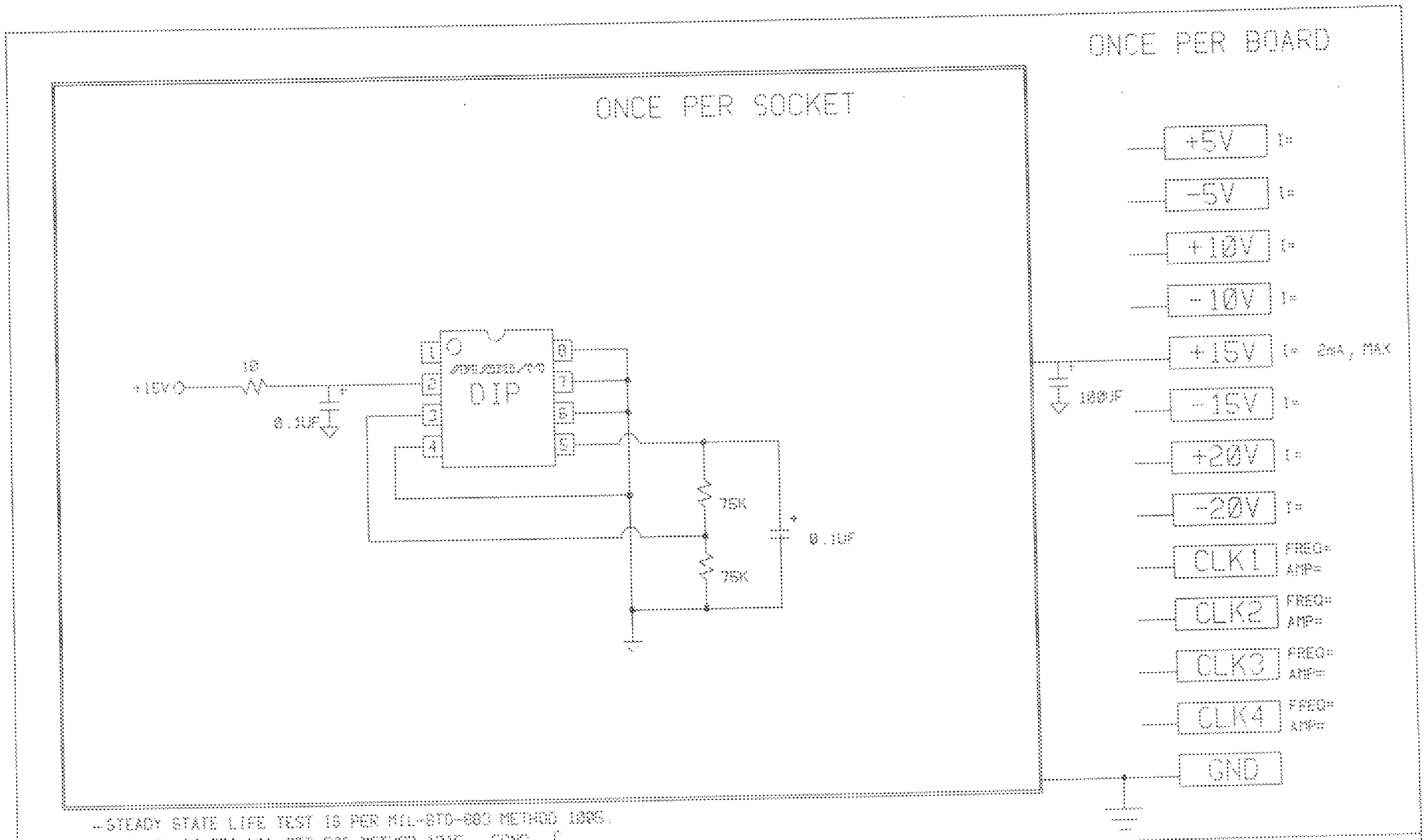
Mil Std 883D
Method 3015.7
Notice 8



PKG.CODE: S8-5		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 95 X 155	PKG. DESIGN			BUILDSHEET NUMBER: 05-1701-0124	REV.: B



PKG.CODE: P8-2		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 110 X 140	PKG. DESIGN			BUILDSHEET NUMBER: 05-1701-0123 / REV.: B



- STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.
- BURN-IN IS PER MIL-STD-883 METHOD 1015. COND. C

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR [X] COMMERCIAL
   [X] MR/883

SPEC. NO. 06-0091 REV. C

DATE: 5/31/95

DRAWN BY:

MAXIM BURN-IN SCHEMATIC

DEVICE TYPE:
MAX770/771/772/1771
MAX808