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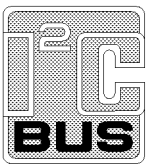


## 1 FEATURES

- I²C-bus interface operating supply voltage: 2.5 V to 6 V
- Clock operating supply voltage (0 to +70 °C): 1.0 V to 6.0 V
- 240 × 8-bit low-voltage RAM
- Data retention voltage: 1.0 V to 6 V
- Operating current (at $f_{SCL}$ = 0 Hz): max. 50 μA
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function
- Slave address:
  - READ: A1 or A3
  - WRITE: A0 or A2.

## 2 GENERAL DESCRIPTION

The PCF8583 is a clock/calendar circuit based on a 2048-bit static CMOS RAM organized as 256 words by 8 bits. Addresses and data are transferred serially via the two-line bidirectional I²C-bus. The built-in word address register is incremented automatically after each written or read data byte. Address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware.

The built-in 32.768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space. The remaining 240 bytes are free RAM locations.

## 3 QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage operating mode | I²C-bus active | 2.5 | – | 6.0 | V |
| | | I²C-bus inactive | 1.0 | – | 6.0 | V |
| $I_{DD}$ | supply current operating mode | $f_{SCL}$ = 100 kHz | – | – | 200 | μA |
| $I_{DDO}$ | supply current clock mode | $f_{SCL}$ = 0 Hz; $V_{DD}$ = 5 V | – | 10 | 50 | μA |
| | | $f_{SCL}$ = 0 Hz; $V_{DD}$ = 1 V | – | 2 | 10 | μA |
| $T_{amb}$ | operating ambient temperature range | | −40 | – | +85 | °C |
| $T_{stg}$ | storage temperature range | | −65 | – | +150 | °C |

## 4 ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| PCF8583P | DIP8 | plastic dual in-line package; 8 leads (300 mil) | SOT97-1 |
| PCF8583T | SO8 | plastic small outline package; 8 leads; body width 7.5 mm | SOT176-1 |

## 5 BLOCK DIAGRAM

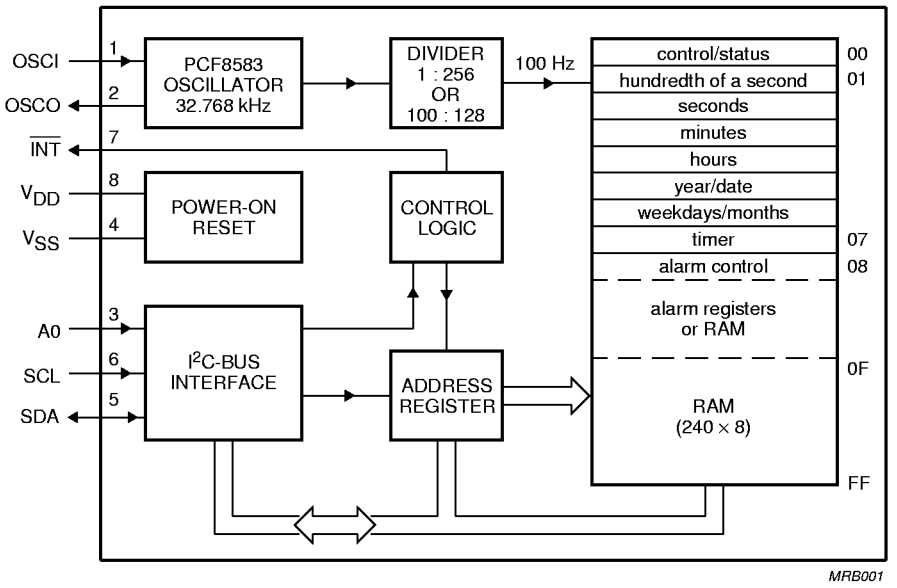



Fig.1 Block diagram.

## 6 PINNING

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| OSCI | 1 | oscillator input, 50 Hz or event-pulse input |
| OSCO | 2 | oscillator output |
| A0 | 3 | address input |
| $V_{SS}$ | 4 | negative supply |
| SDA | 5 | serial data line |
| SCL | 6 | serial clock line |
| $\overline{INT}$ | 7 | open drain interrupt output (active LOW) |
| $V_{DD}$ | 8 | positive supply |

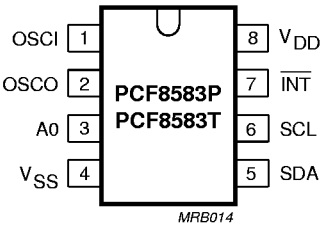



Fig.2 Pinning diagram.

## 7 FUNCTIONAL DESCRIPTION

The PCF8583 contains a 256 by 8-bit RAM with an 8-bit auto-increment address register, an on-chip 32.768 kHz oscillator circuit, a frequency divider, a serial two-line bidirectional $I^2C$-bus interface and a power-on reset circuit.

The first 16 bytes of the RAM (memory addresses 00 to 0F) are designed as addressable 8-bit parallel special function registers. The first register (memory address 00) is used as a control/status register. The memory addresses 01 to 07 are used as counters for the clock function. The memory addresses 08 to 0F may be programmed as alarm registers or used as free RAM locations, when the alarm is disabled.

### 7.1 Counter function modes

When the control/status register is programmed, a 32.768 kHz clock mode, a 50 Hz clock mode or an event-counter mode can be selected.

In the clock modes the hundredths of a second, seconds, minutes, hours, date, month (four year calendar) and weekday are stored in a BCD format. The timer register stores up to 99 days. The event counter mode is used to count pulses applied to the oscillator input (OSCO left open-circuit). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01 to 07), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore, faulty reading of the count during a carry condition is prevented.

When a counter is written, other counters are not affected.

### 7.2 Alarm function modes

By setting the alarm enable bit of the control/status register the alarm control register (address 08) is activated.

By setting the alarm control register a dated alarm, a daily alarm, a weekday alarm or a timer alarm may be programmed. In the clock modes, the timer register (address 07) may be programmed to count hundredths of a second, seconds, minutes, hours or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control/status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open drain interrupt output is switched on (active LOW) when the alarm or timer flag is set (enabled). The flags remain set until directly reset by a write operation.

When the alarm is disabled (Bit 2 of control/status register = 0) the alarm registers at addresses 08 to 0F may be used as free RAM.

### 7.3 Control/status register

The control/status register is defined as the memory location 00 with free access for reading and writing via the $I^2C$-bus. All functions and options are controlled by the contents of the control/status register (see Fig.3).

### 7.4 Counter registers

In the clock modes 24 h or 12 h format can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in Fig.5.

The year and date are packed into memory location 05 (see Fig.6). The weekdays and months are packed into memory location 06 (see Fig.7). When reading these memory locations the year and weekdays are masked out when the mask flag of the control/status register is set. This allows the user to read the date and month count directly.

In the event-counter mode events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is by-passed.

In the different modes the counter registers are programmed and arranged as shown in Fig.4. Counter cycles are listed in Table 1.

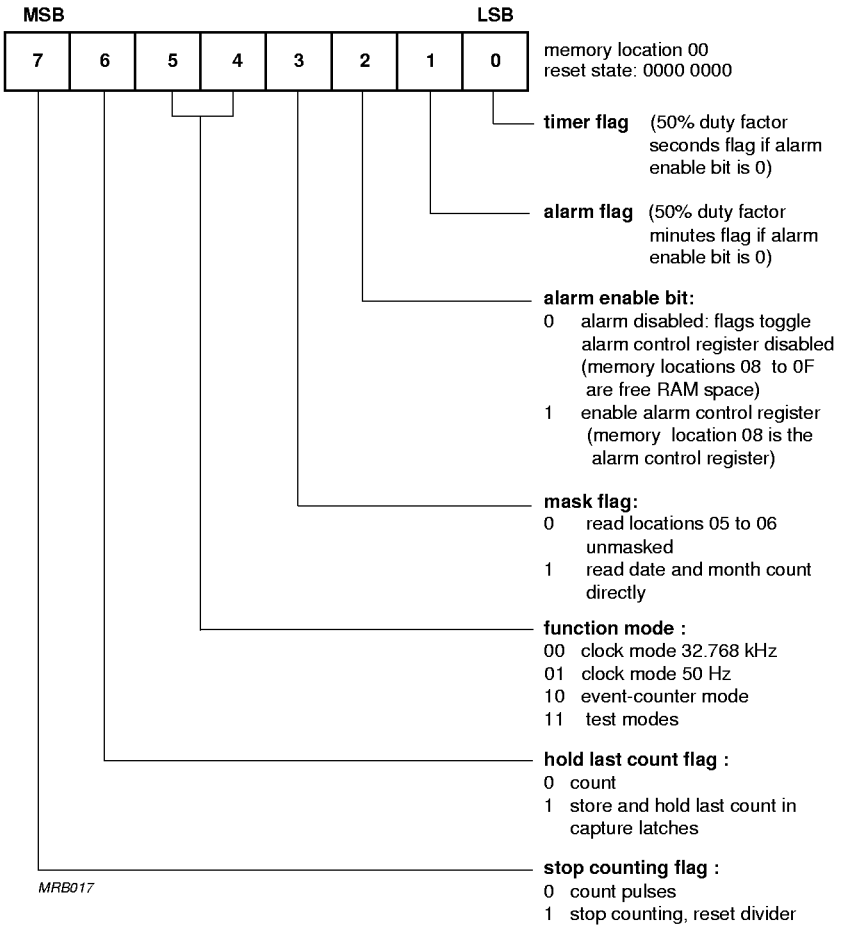



Fig.3 Control/status register.

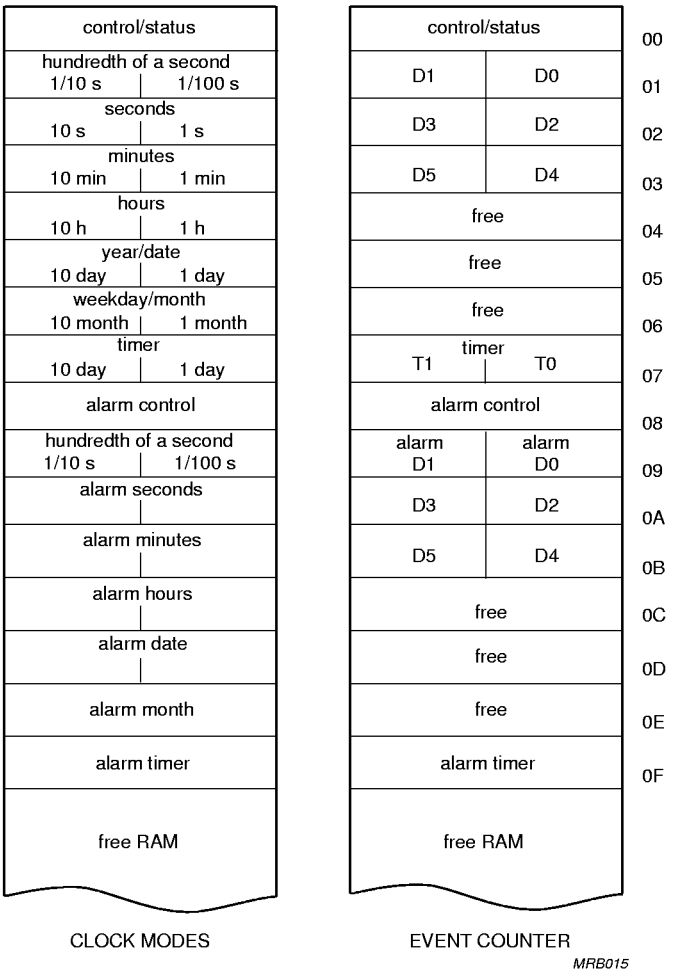



Fig.4 Register arrangement.

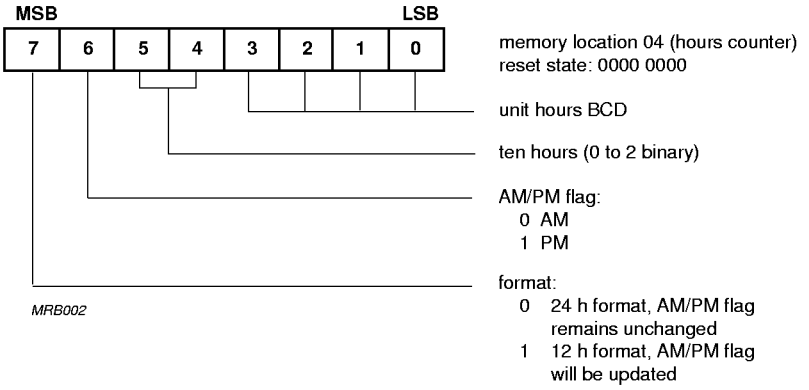



Fig.5 Format of the hours counter.

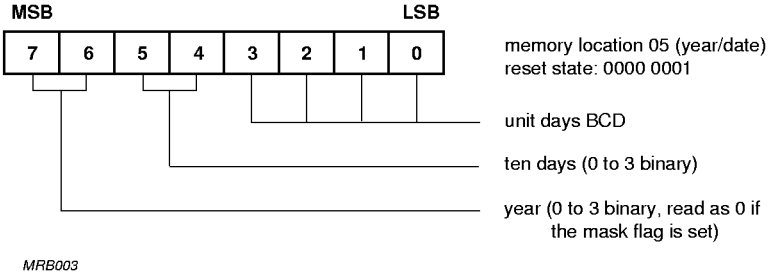



Fig.6 Format of the year/date counter.

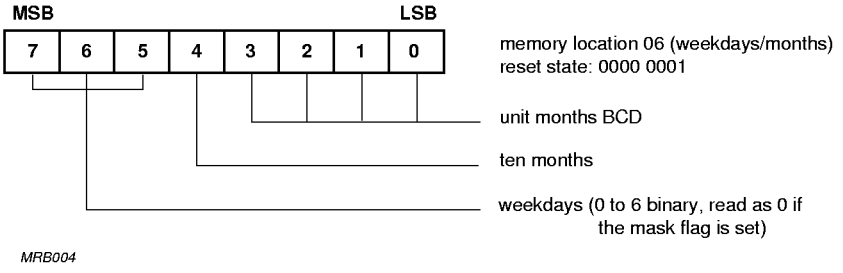



Fig.7 Format of the weekdays/month counter.

**Table 1** Cycle length of the time counters, clock modes

| UNIT | COUNTING CYCLE | CARRY TO NEXT UNIT | CONTENTS OF THE MONTH COUNTER |
|---|---|---|---|
| Hundredths of a second | 00 to 99 | 99 to 00 | – |
| Seconds | 00 to 59 | 59 to 00 | – |
| Minutes | 00 to 59 | 59 to 00 | – |
| Hours (24 h) | 00 to 23 | 23 to 00 | – |
| Hours (12 h) | 12 AM | – | – |
| | 01 AM to 11 AM | – | – |
| | 12 PM | – | – |
| | 01 PM to 11 PM | 11 PM to 12 AM | – |
| Date | 01 to 31 | 31 to 01 | 1, 3, 5, 7, 8, 10 and 12 |
| | 01 to 30 | 30 to 01 | 4, 6, 9 and 11 |
| | 01 to 29 | 29 to 01 | 2, year = 0 |
| | 01 to 28 | 28 to 01 | 2, year = 1, 2 and 3 |
| Months | 01 to 12 | 12 to 01 | – |
| Year | 0 to 3 | – | – |
| Weekdays | 0 to 6 | 6 to 0 | – |
| Timer | 00 to 99 | no carry | – |

### 7.5 Alarm control register

When the alarm enable bit of the control/status register is set (address 00, bit 2) the alarm control register (address 08) is activated. All alarm, timer, and interrupt output functions are controlled by the contents of the alarm control register (see Fig.8).

### 7.6 Alarm registers

All alarm registers are allocated with a constant address offset of hexadecimal 08 to the corresponding counter registers (see Fig.4, Register arrangement).

An alarm signal is generated when the contents of the alarm registers matches bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected, the contents of the alarm weekday/month register will select the weekdays on which an alarm is activated (see Fig.9).

**Remark**: In the 12 h mode, bits 6 and 7 of the alarm hours register must be the same as the hours counter.

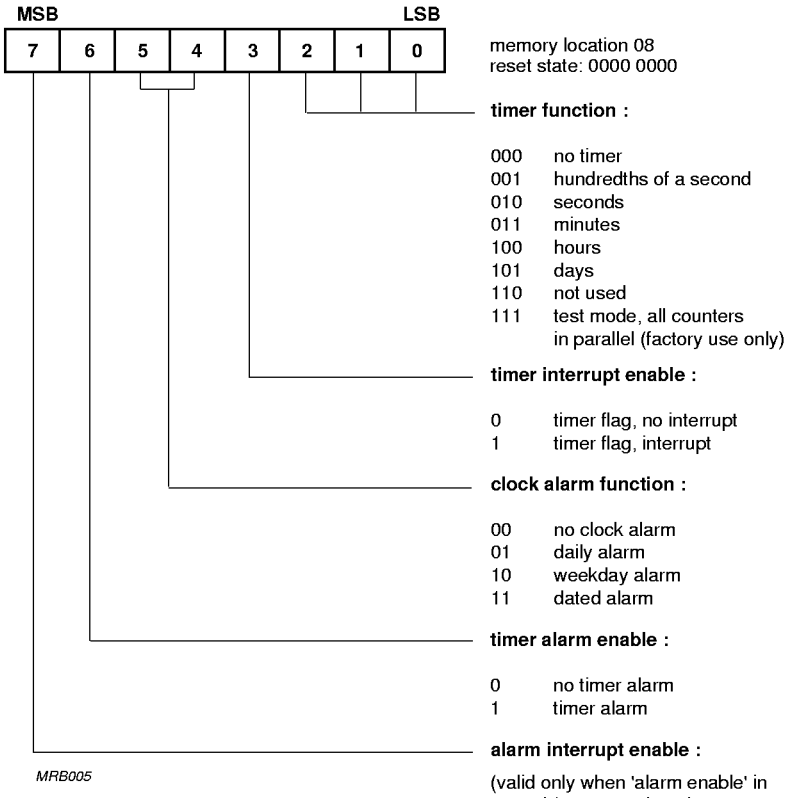



Fig.8 Alarm control register; clock mode.

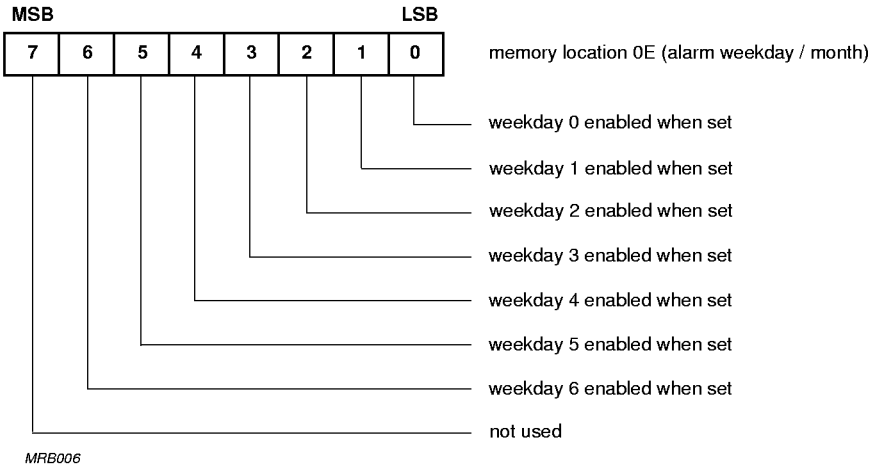



Fig.9 Selection of alarm weekdays.

### 7.7 Timer

The timer (location 07) is enabled by setting the control/status register = XX0X X1XX. The timer counts up from 0 (or a programmed value) to 99. On overflow, the timer resets to 0. The timer flag (LSB of control/status register) is set on overflow of the timer. This flag must be reset by software. The inverted value of this flag can be transferred to the external interrupt by setting bit 3 of the alarm control register.

Additionally, a timer alarm can be programmed by setting the timer alarm enable (bit 6 of the alarm control register). When the value of the timer equals a pre-programmed value in the alarm timer register (location 0F), the alarm flag is set (bit 1 of the control/status register). The inverted value of the alarm flag can be transferred to the external interrupt by enabling the alarm interrupt (bit 6 of the alarm control register).

Resolution of the timer is programmed via the 3 LSBs of the alarm control register (see Fig.11, Alarm and timer Interrupt logic diagram).

### 7.8 Event counter mode

Event counter mode is selected by bits 4 and 5 which are logic 1, 0 in the control/status register. The event counter mode is used to count pulses externally applied to the oscillator input (OSCO left open-circuit).

The event counter stores up to 6 digits of data, which are stored as 6 hexadecimal values located in locations 1, 2, and 3. Thus, up to 1 million events may be recorded.

An event counter alarm occurs when the event counter registers match the value programmed in locations 9, A, and B, and the event alarm is enabled (bits 4 and 5 which are logic 0, 1 in the alarm control register). In this event, the alarm flag (bit 1 of the control/status register) is set. The inverted value of this flag can be transferred to the interrupt pin (pin 7) by setting the alarm interrupt enable in the alarm control register. In this mode, the timer (location 07) increments once for every one, one-hundred, ten thousand, or 1 million events, depending on the value programmed in bits 0, 1 and 2 of the alarm control register. In all other events, the timer functions are as in the clock mode.

### 7.9 Interrupt output

The conditions for activating the open-drain n-channel interrupt output $\overline{INT}$ (active LOW) are determined by appropriate programming of the alarm control register. These conditions are clock alarm, timer alarm, timer overflow, and event counter alarm. An interrupt occurs when the alarm flag or the timer flag is set, and the corresponding interrupt is enabled. In all events, the interrupt is cleared only by software resetting of the flag which initiated the interrupt.

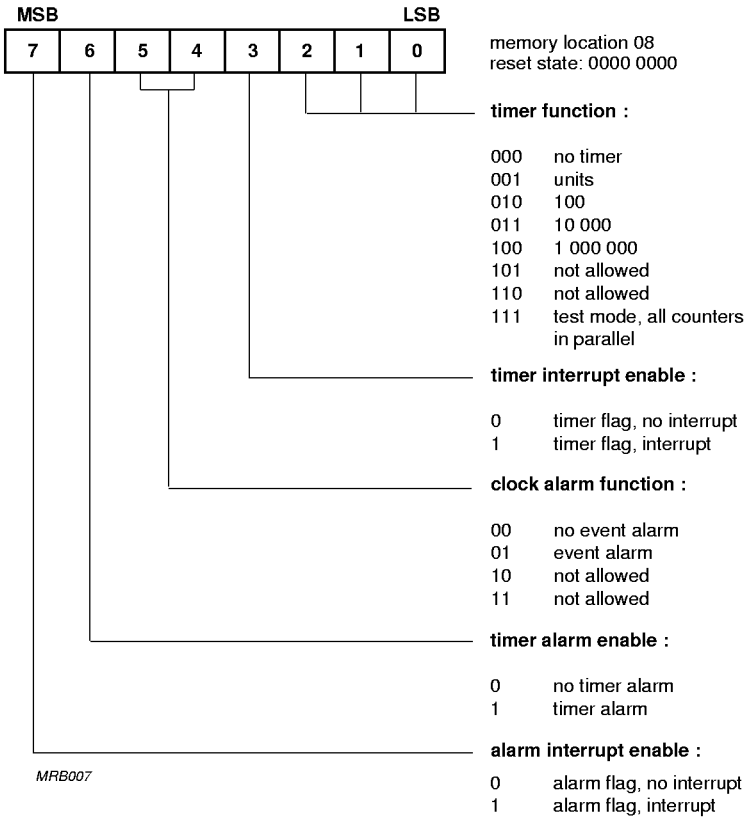



Fig.10 Alarm control register, event-counter mode.

In the clock mode, if the alarm enable is not activated (alarm enable bit of control/status register is logic 0), the interrupt output toggles at 1 Hz with a 50% duty cycle (may be used for calibration). This is the default power-on state of the device. The OFF voltage of the interrupt output may exceed the supply voltage, up to a maximum of 6.0 V. A logic diagram of the interrupt output is shown in Fig.11.

### 7.10 Oscillator and divider

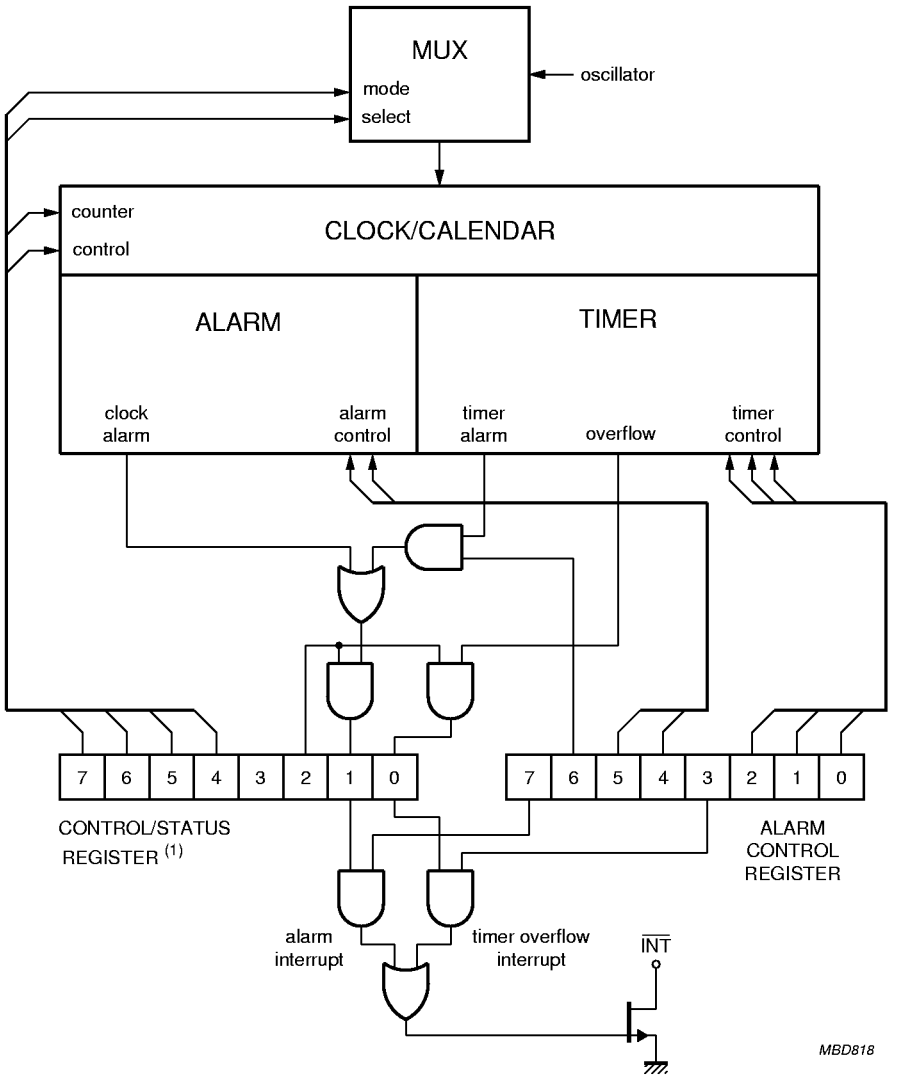
A 32.768 kHz quartz crystal has to be connected to OSCI (pin 1) and OSCO (pin 2). A trimmer capacitor between OSCI and $V_{DD}$ is used for tuning the oscillator (see quartz frequency adjustment). A 100 Hz clock signal is derived from the quartz oscillator for the clock counters.

In the 50 Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high impedance state. This allows the user to feed the 50 Hz reference frequency or an external high speed event signal into the input OSCI.

### 7.11 Initialization

When power-up occurs the $I^2C$-bus interface, the control/status register and all clock counters are reset. The device starts time-keeping in the 32.768 kHz clock mode with the 24 h format on the first of January at 0.00.00: 00. A 1 Hz square wave with 50% duty cycle appears at the interrupt output pin (starts HIGH).

It is recommended to set the stop counting flag of the control/status register before loading the actual time into the counters. Loading of illegal states may lead to a temporary clock malfunction.




(1) If the alarm enable bit of the control/status register is reset (logic 0), a 1 Hz signal can be observed on the interrupt pin $\overline{INT}$.

Fig.11 Alarm and timer interrupt logic diagram.

## 8 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

### 8.1 Bit transfer (see Fig.12)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

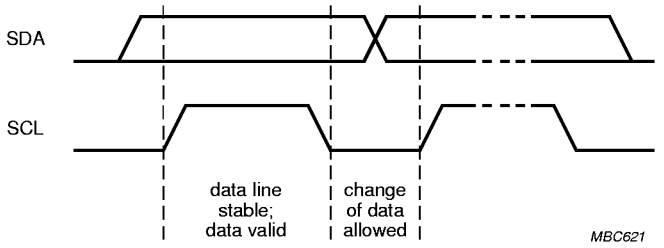



Fig.12 Bit transfer.

### 8.2 Start and stop conditions (see Fig.13)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

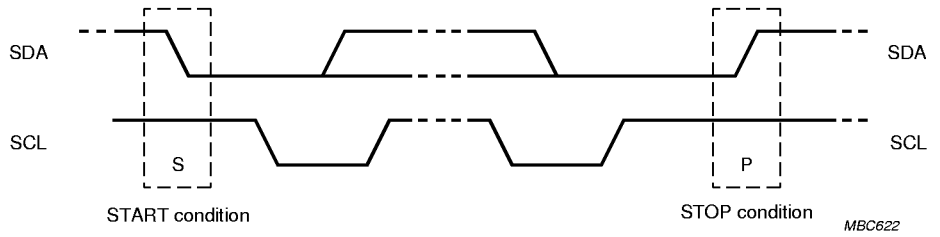



Fig.13 Definition of start and stop conditions.

### 8.3 System configuration (see Fig.14)

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

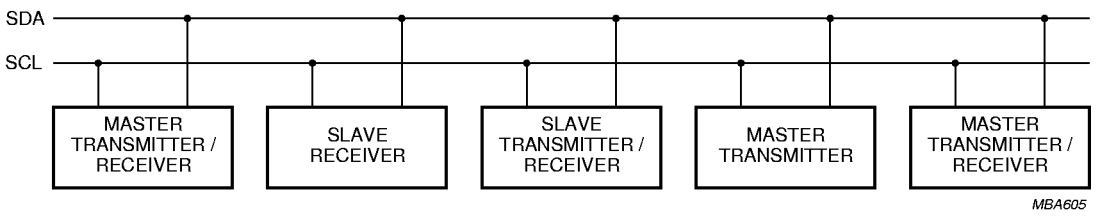



Fig.14 System configuration.

### 8.4 Acknowledge (see Fig.15)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

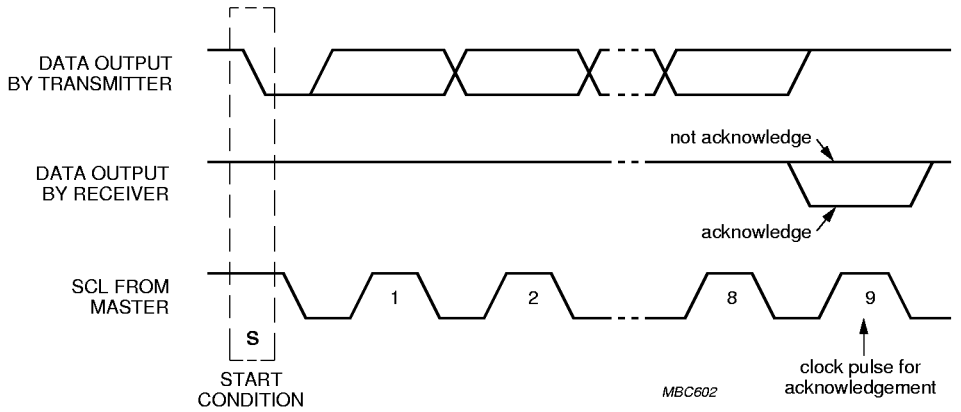



Fig.15 Acknowledgment on the $I^2C$-bus.

## 9 I²C-BUS PROTOCOL

### 9.1 Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

The clock/calendar slave address is shown in Fig.16. Bit A0 corresponds to hardware address pin A0. Connecting this pin to $V_{DD}$ or $V_{SS}$ allows the device to have one of two different addresses.

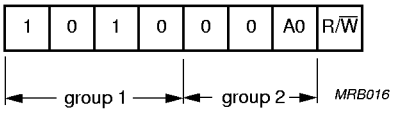



Fig.16 Slave address.

### 9.2 Clock/calendar READ/WRITE cycles

The I²C-bus configuration for the different PCF8583 READ and WRITE cycles is shown in Figs 17, 18 and 19.

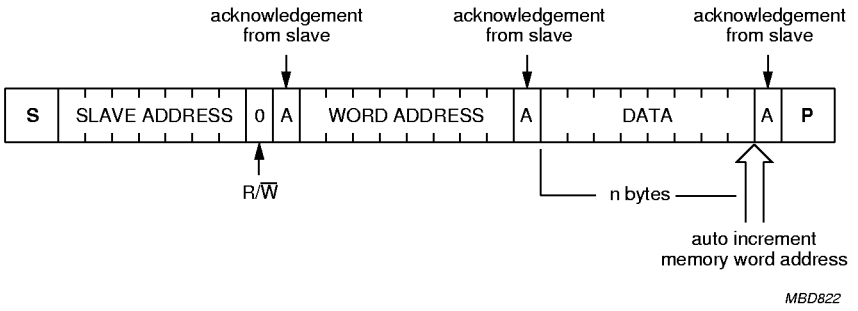



Fig.17 Master transmits to slave receiver (WRITE) mode.

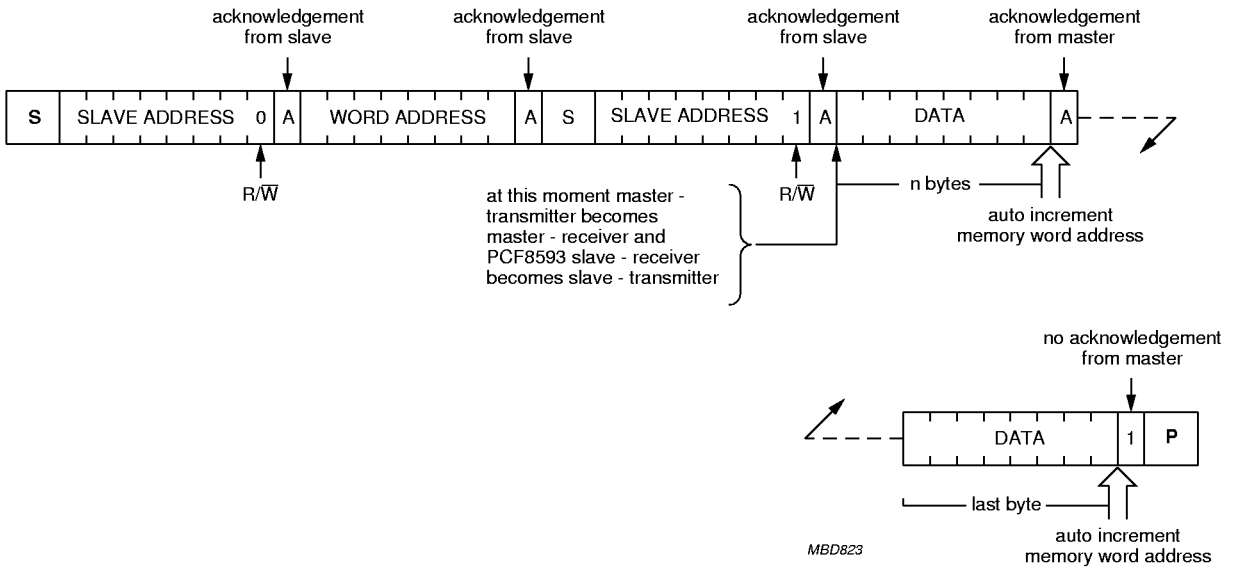



Fig.18 Master reads after setting word address (write word address; READ data).

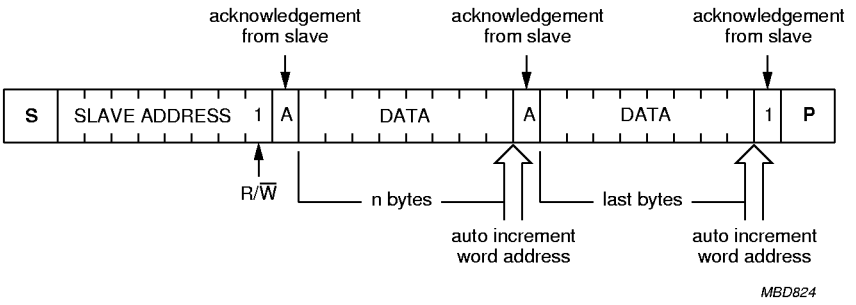



Fig.19 Master reads slave immediately after first byte (READ mode).

## 10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | supply voltage (pin 8) | –0.8 | +7.0 | V |
| $I_{DD}$ | supply current (pin 8) | – | 50 | mA |
| $I_{SS}$ | supply current (pin 4) | – | 50 | mA |
| $V_I$ | input voltage | –0.8 | $V_{DD}$ + 0.8 | V |
| $I_I$ | DC input current | – | 10 | mA |
| $I_O$ | DC output current | – | 10 | mA |
| $P_{tot}$ | total power dissipation per package | – | 300 | mW |
| $P_O$ | power dissipation per output | – | 50 | mW |
| $T_{amb}$ | operating ambient temperature | –40 | +85 | °C |
| $T_{stg}$ | storage temperature | –65 | +150 | °C |

## 11 HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC12 under *"Handling MOS Devices"*.

## 12 DC CHARACTERISTICS

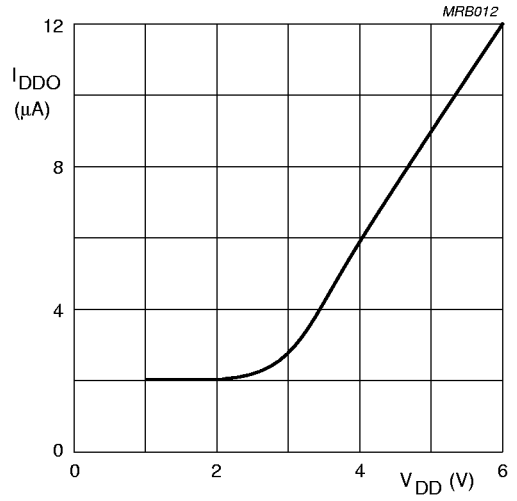
$V_{DD}$ = 2.5 to 6.0 V; $V_{SS}$ = 0 V; $T_{amb}$ = –40 to +85 °C unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP.(1) | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage (operating mode) | I²C-bus active | 2.5 | – | 6.0 | V |
| | | I²C-bus inactive | 1.0 | – | 6.0 | V |
| $V_{DDosc}$ | supply voltage (quartz oscillator) | $T_{amb}$ = 0 to 70 °C; note 2 | 1.0 | – | 6.0 | V |
| $I_{DD}$ | supply current (operating mode) | $f_{SCL}$ = 100 kHz; clock mode; note 3 | – | – | 200 | µA |
| $I_{DDO}$ | supply current (clock mode) | see Fig.20 | | | | |
| | | $f_{SCL}$ = 0 Hz; $V_{DD}$ = 5 V | – | 10 | 50 | µA |
| | | $f_{SCL}$ = 0 Hz; $V_{DD}$ = 1 V | – | 2 | 10 | µA |
| $I_{DDR}$ | data retention | $f_{OSCI}$ = 0 Hz; $V_{DD}$ = 1 V | | | | |
| | | $T_{amb}$ = –40 to + 85 °C | – | – | 5 | µA |
| | | $T_{amb}$ = –25 to + 70 °C | – | – | 2 | µA |
| $V_{EN}$ | I²C-bus enable level | note 4 | 1.5 | 1.9 | 2.3 | V |
| **SDA** | | | | | | |
| $V_{IL}$ | LOW level input voltage | note 5 | –0.8 | – | $0.3V_{DD}$ | V |
| $V_{IH}$ | HIGH level input voltage | note 5 | $0.7V_{DD}$ | – | $V_{DD}$ +0.8 | V |
| $I_{OL}$ | LOW level output current | $V_{OL}$ = 0.4 V | 3 | – | – | mA |
| $I_{LI}$ | input leakage current | $V_I = V_{DD}$ or $V_{SS}$ | –1 | – | +1 | µA |
| $C_i$ | input capacitance | note 6 | – | – | 7 | pF |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP.(1) | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **A0; OSCI** | | | | | | |
| $I_{LI}$ | input leakage current | $V_I = V_{DD}$ or $V_{SS}$ | −250 | – | +250 | nA |
| **$\overline{INT}$** | | | | | | |
| $I_{OL}$ | LOW level output current | $V_{OL}$ = 0.4 V | 3 | – | – | mA |
| $I_{LI}$ | input leakage current | $V_I = V_{DD}$ or $V_{SS}$ | −1 | – | +1 | µA |
| **SCL** | | | | | | |
| $C_i$ | input capacitance | note 6 | – | – | 7 | pF |
| $I_{LI}$ | input leakage current | $V_I = V_{DD}$ or $V_{SS}$ | −1 | – | +1 | µA |

**Notes**

1. Typical values measured at $T_{amb}$ = 25 °C.
2. When powering-up the device, $V_{DD}$ must exceed 1.5 V until stable operation of the oscillator is established.
3. Event counter mode: supply current dependant upon input frequency.
4. The $I^2C$-bus logic is disabled if $V_{DD} < V_{EN}$.
5. When the voltages are above or below the supply voltages $V_{DD}$ or $V_{SS}$, an input current may flow; this current must not exceed ±0.5 mA.
6. Tested on sample basis.




$f_{SCL}$ = 32 kHz; $T_{amb}$ = 25 °C.

Fig.20 Typical supply current in clock mode as a function of supply voltage.

## 13 AC CHARACTERISTICS

$V_{DD}$ = 2.5 to 6.0 V; $V_{SS}$ = 0 V; $T_{amb}$ = –40 to +85 °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Oscillator** | | | | | | |
| $C_{osc}$ | integrated oscillator capacitance | | – | 40 | – | pF |
| $\Delta f_{osc}$ | oscillator stability | for $\Delta V_{DD}$ = 100 mV; $T_{amb}$ = 25 °C; $V_{DD}$ = 1.5 V | – | $2 \times 10^{-7}$ | – | |
| $f_i$ | input frequency | note 1 | – | – | 1 | MHz |
| **Quartz crystal parameters (f = 32.768 kHz)** | | | | | | |
| $R_s$ | series resistance | | – | – | 40 | kΩ |
| $C_L$ | parallel load capacitance | | – | 10 | – | pF |
| $C_T$ | trimmer capacitance | | 5 | – | 25 | pF |
| **I²C-bus timing** (see Fig.21; notes 2 and 3) | | | | | | |
| $f_{SCL}$ | SCL clock frequency | | – | – | 100 | kHz |
| $t_{SP}$ | tolerable spike width on bus | | – | – | 100 | ns |
| $t_{BUF}$ | bus free time | | 4.7 | – | – | µs |
| $t_{SU;STA}$ | START condition set-up time | | 4.7 | – | – | µs |
| $t_{HD;STA}$ | START condition hold time | | 4.0 | – | – | µs |
| $t_{LOW}$ | SCL LOW time | | 4.7 | – | – | µs |
| $t_{HIGH}$ | SCL HIGH time | | 4.0 | – | – | µs |
| $t_r$ | SCL and SDA rise time | | – | – | 1.0 | µs |
| $t_f$ | SCL and SDA fall time | | – | – | 0.3 | µs |
| $t_{SU;DAT}$ | data set-up time | | 250 | – | – | ns |
| $t_{HD;DAT}$ | data hold time | | 0 | – | – | ns |
| $t_{VD;DAT}$ | SCL LOW to data out valid | | – | – | 3.4 | µs |
| $t_{SU;STO}$ | STOP condition set-up time | | 4.0 | – | – | µs |

**Notes**

1. Event counter mode only.
2. All timing values are valid within the operating supply voltage and ambient temperature range and reference to $V_{IL}$ and $V_{IH}$ with an input voltage swing of $V_{SS}$ to $V_{DD}$.
3. A detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

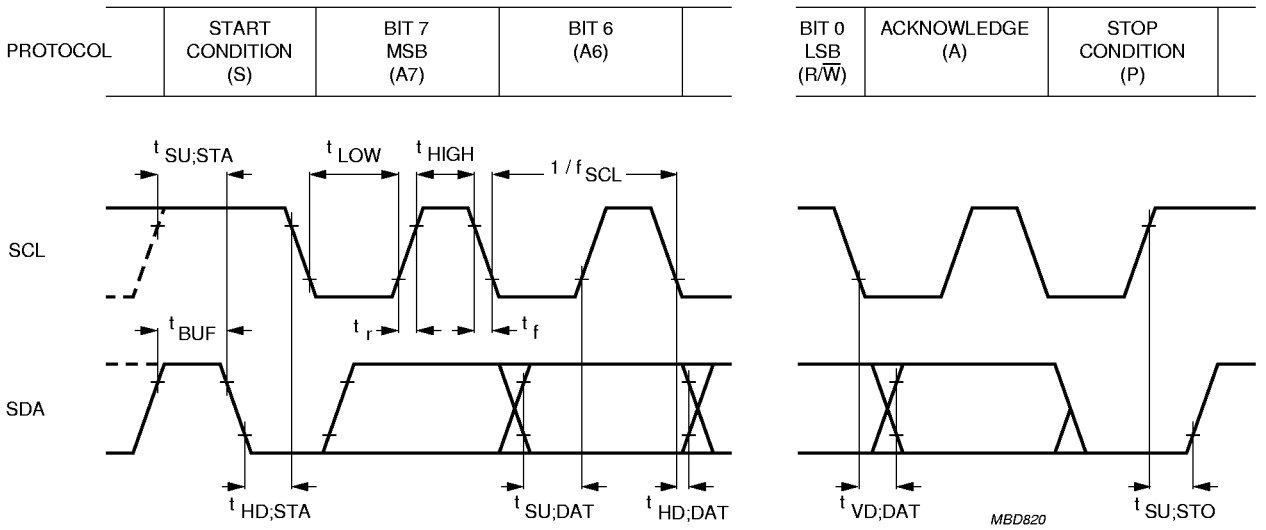



Fig.21 I²C-bus timing diagram; rise and fall times refer to $V_{IL}$ and $V_{IH}$.

## 14 APPLICATION INFORMATION

### 14.1 Quartz frequency adjustment

#### 14.1.1 METHOD 1: FIXED OSCI CAPACITOR

By evaluating the average capacitance necessary for the application layout a fixed capacitor can be used.
The frequency is best measured via the 1 Hz signal available after power-on at the interrupt output (pin 7).
The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average $\pm 5 \times 10^{-6}$).
Average deviations of ±5 minutes per year can be achieved.

#### 14.1.2 METHOD 2: OSCI TRIMMER

Using the alarm function (via the I²C-bus) a signal faster than 1 Hz can be generated at the interrupt output for fast setting of a trimmer.

Procedure:

- Power-on
- Initialization (alarm functions).

Routine:

- Set clock to time T and set alarm to time T + dT
- At time T + dT (interrupt) repeat routine.

#### 14.1.3 METHOD 3:

Direct measurement of OSC out (accounting for test probe capacitance).

The PCF8583 slave address has a fixed combination 1010 as group 1.

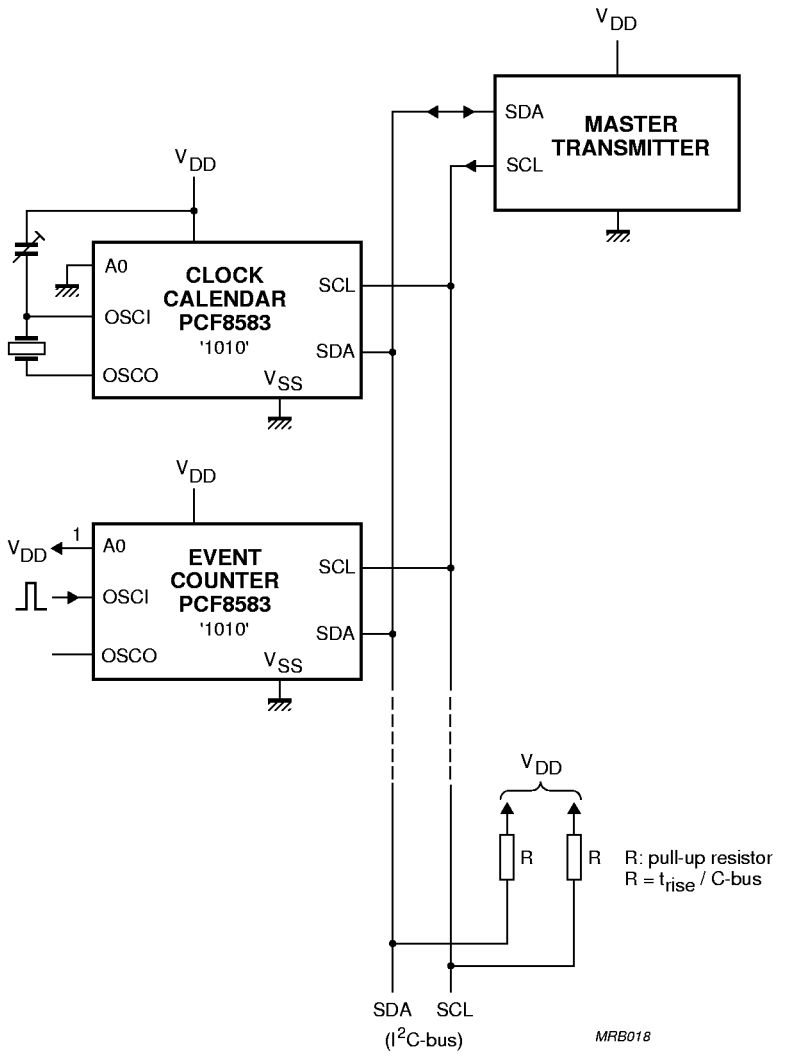
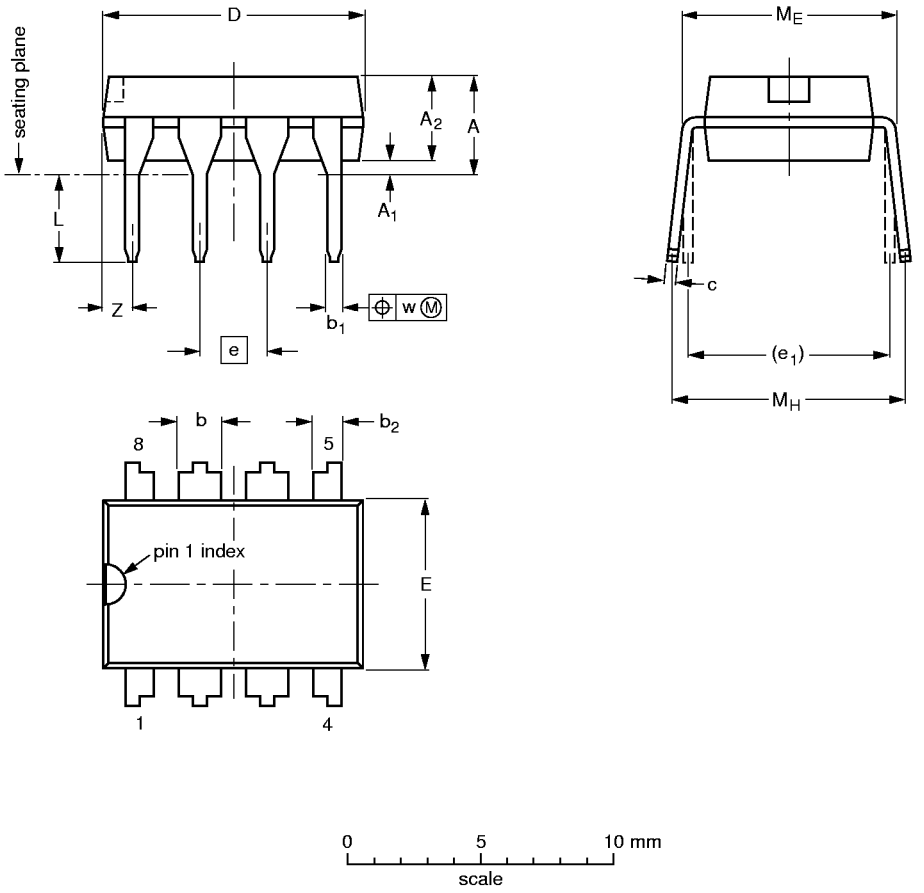



Fig.22 Application diagram.

## 15 PACKAGE OUTLINES

**DIP8: plastic dual in-line package; 8 leads (300 mil)** **SOT97-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

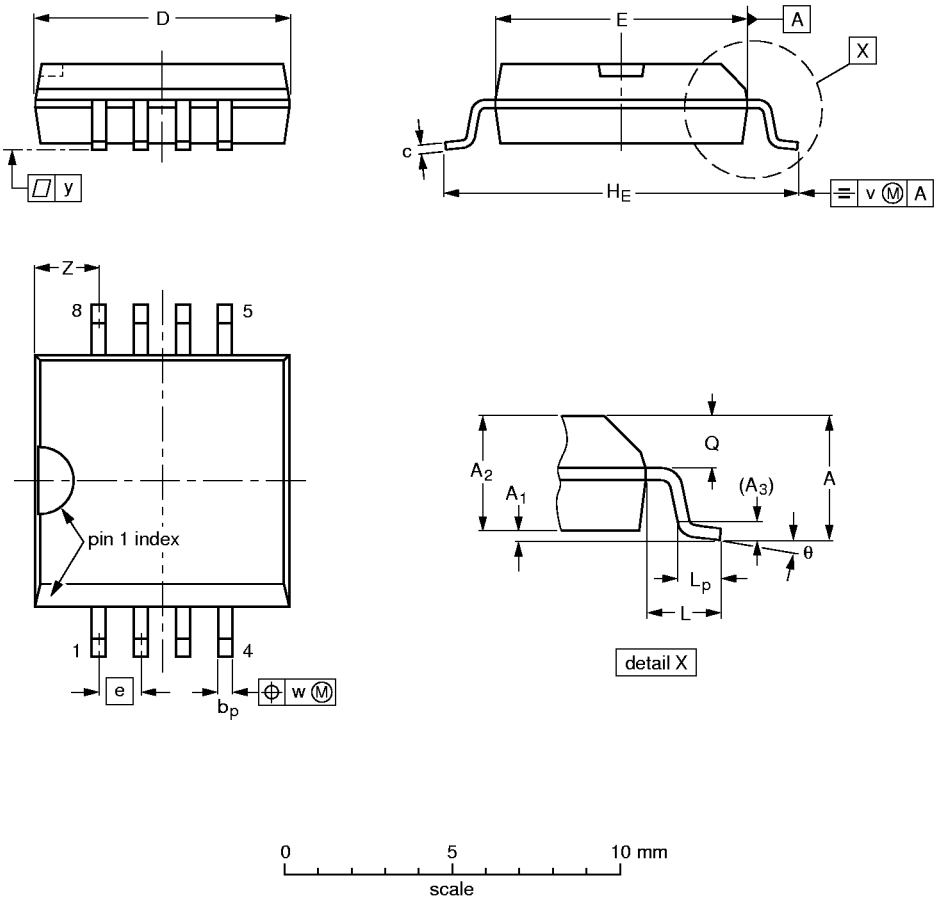
| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | $b_2$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.2 | 0.51 | 3.2 | 1.73<br>1.14 | 0.53<br>0.38 | 1.07<br>0.89 | 0.36<br>0.23 | 9.8<br>9.2 | 6.48<br>6.20 | 2.54 | 7.62 | 3.60<br>3.05 | 8.25<br>7.80 | 10.0<br>8.3 | 0.254 | 1.15 |
| inches | 0.17 | 0.020 | 0.13 | 0.068<br>0.045 | 0.021<br>0.015 | 0.042<br>0.035 | 0.014<br>0.009 | 0.39<br>0.36 | 0.26<br>0.24 | 0.10 | 0.30 | 0.14<br>0.12 | 0.32<br>0.31 | 0.39<br>0.33 | 0.01 | 0.045 |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT97-1 | 050G01 | MO-001AN | | | | ~~92-11-17~~<br>95-02-04 |

**SO8: plastic small outline package; 8 leads; body width 7.5 mm** **SOT176-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.3<br>0.1 | 2.45<br>2.25 | 0.25 | 0.49<br>0.36 | 0.32<br>0.23 | 7.65<br>7.45 | 7.6<br>7.4 | 1.27 | 10.65<br>10.00 | 1.45 | 1.1<br>0.45 | 1.1<br>1.0 | 0.25 | 0.25 | 0.1 | 2.0<br>1.8 | 8°<br>0° |
| inches | 0.10 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.019<br>0.014 | 0.013<br>0.009 | 0.30<br>0.29 | 0.30<br>0.29 | 0.050 | 0.419<br>0.394 | 0.057 | 0.043<br>0.018 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.079<br>0.071 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT176-1 | | | | | | ~~95-02-25~~<br>97-05-22 |

## 16 SOLDERING

### 16.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

### 16.2 DIP

#### 16.2.1 SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

#### 16.2.2 REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

### 16.3 SO

#### 16.3.1 REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

#### 16.3.2 WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### 16.3.3 REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.