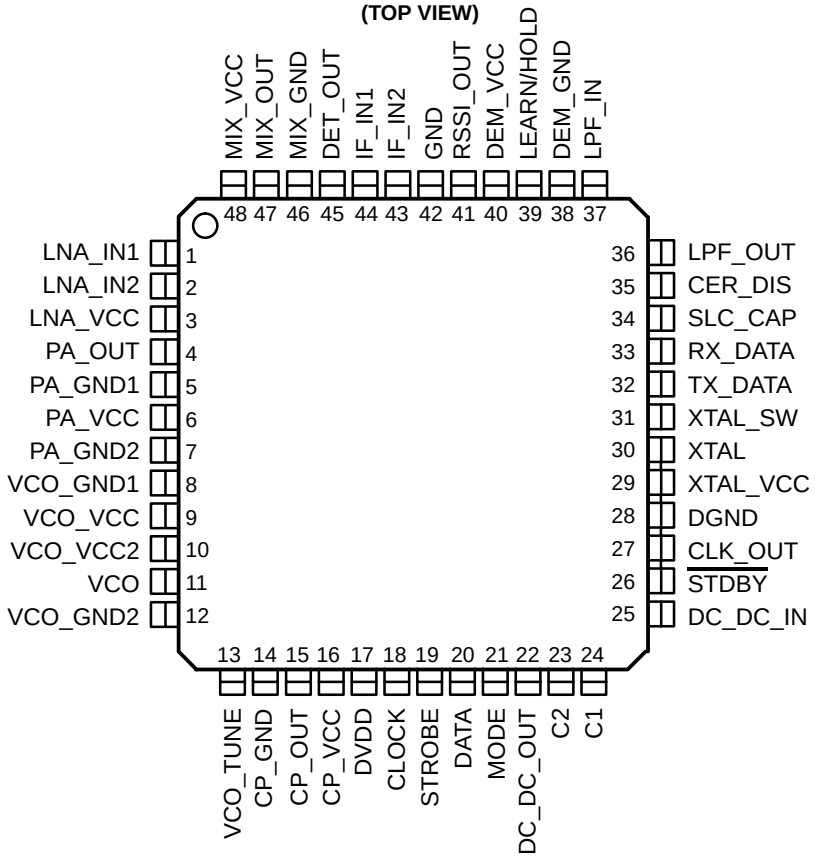
- **Single-Chip RF Transceiver for 868-MHz and 915-MHz Industrial, Scientific, and Medical (ISM) Bands**
- **1.8-V to 3.6-V Operation**
- **860-MHz to 930-MHz Operation**
- **Low Power Consumption**
- **FSK/OOK Operation**
- **Integer-N Synthesizer With Fully Integrated Voltage Controlled Oscillator (VCO)**
- **On-Chip Reference Oscillator and Phase-Locked Loop (PLL)**
- **9-dBm Typical Output Power**
- **Programmable Brownout Detector**
- **Linear Receive Strength Signal Indicator (RSSI)**
- **Flexible 3-Wire Serial Interface**
- **Minimal Number of External Components Required**
- **48-Pin Low-Profile Plastic Quad Flat Package (PQFP)**
- **Programmable XTAL Trimming**

PQFP PACKAGE
(TOP VIEW)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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description

The TRF6901 single-chip solution is an integrated circuit intended for use as a low cost FSK or OOK transceiver to establish a frequency-programmable, half-duplex, bidirectional RF link. The multichannel transceiver is intended for digital (FSK, OOK) modulated applications in the new 868-MHz European band and the North American 915-MHz ISM band. The single-chip transceiver operates down to 1.8 V and is designed for low power consumption. The synthesizer has a typical channel spacing of better than 200 kHz and uses a fully-integrated VCO. Only the PLL loop filter is external to the device.

Two fully-programmable operation modes, Mode0 and Mode1, allow extremely fast switching between two preprogrammed settings (for example, receive (RX)/transmit (TX); TX_frequency_0/TX_frequency_1; RX_frequency_0/RX_frequency_1; …) without reprogramming the device.

ISM band standards

Europe has assigned an unlicensed frequency band of 868 MHz to 870 MHz. This band is specifically defined for short range devices with duty cycles from 0.1% to 100% in several subbands. The existing 433-MHz band for short-range devices in Europe has the great disadvantage of high usage. The new European frequency band, due to the duty cycle assignment, allows a reliable RF link and makes many new applications possible.

The North American unlicensed ISM band covers 902 MHz to 928 MHz (center frequency of 915 MHz) and is suitable for short range RF links.

transmitter

The transmitter consists of an integrated VCO and tank circuit, a complete integer-N synthesizer, and a power amplifier. The divider, prescaler, and reference oscillator require only the addition of an external crystal and a loop filter to provide a complete PLL with a typical frequency resolution of better than 200 kHz.

Since the typical RF output power is approximately 9 dBm, no additional external RF power amplifier is necessary in most applications.

receiver

The integrated receiver is intended to be used as a single-conversion FSK/OOK receiver. It consists of a low noise amplifier, mixer, limiter, FM/FSK demodulator with an external LC tank circuit or ceramic resonator, a LPF amplifier, and a data slicer. The received strength signal indicator (RSSI) can be used for fast carrier sense detection or as an on/off keying, or amplitude shift keying, (OOK/ASK) demodulator.

baseband interface

The TRF6901 can easily be interfaced to a baseband processor such as the Texas Instruments MSP430 ultralow-power microcontroller (see Figure 1). The TRF6901 serial control registers are programmed by the MSP430 and the MSP430 performs baseband operations in the software.

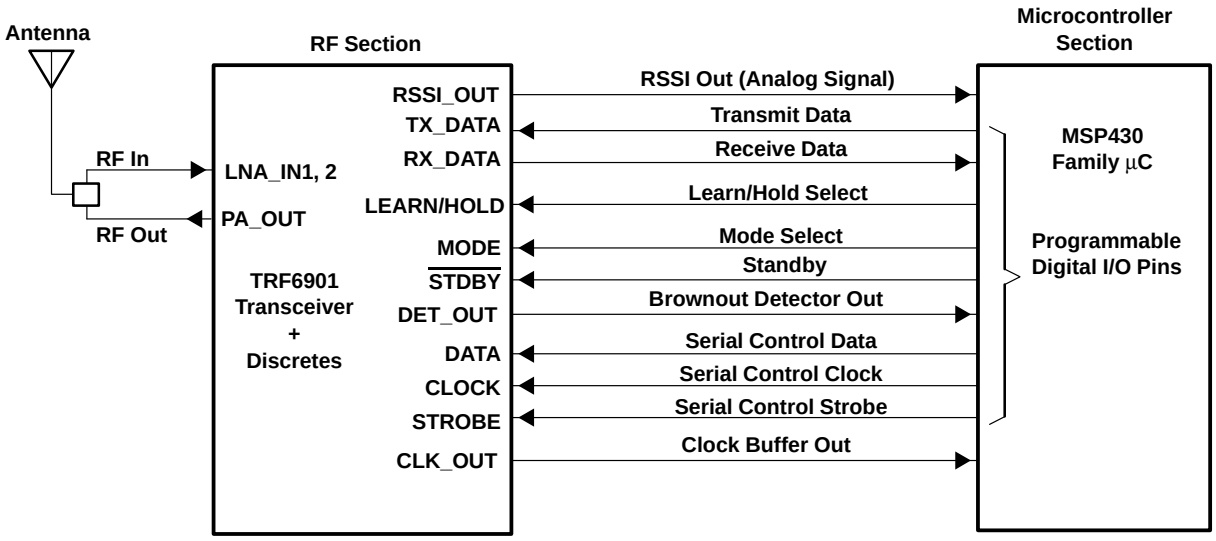
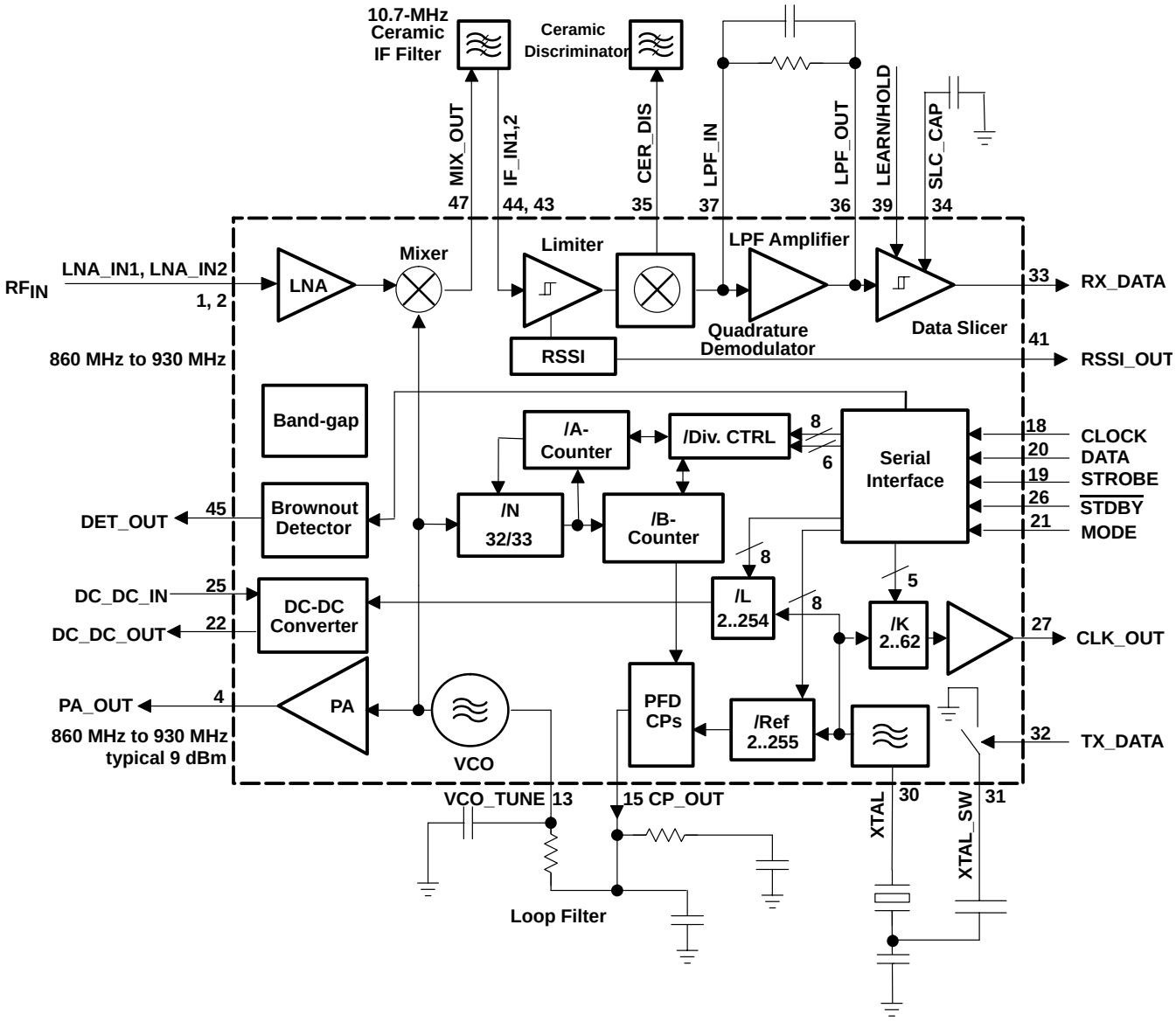


Figure 1. System Block Diagram for Interfacing to the MSP430 Microcontroller

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
C1	24		Connect to external capacitor for operation of dc-dc converter
C2	23		Connect to external capacitor for operation of dc-dc converter
CER_DIS	35		Connect to external ceramic discriminator
CLK_OUT	27	O	Clock signal output for connection to external microcontroller
CLOCK	18	I	Serial interface clock signal input
CP_GND	14		Charge pump ground
CP_OUT	15	O	Charge pump output
CP_VCC	16	I	Charge pump input V_{CC} from dc-dc converter
DATA	20	I	Serial interface data signal input

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DC_DC_IN	25	I	Input to dc-dc converter
DC_DC_OUT	22	O	Output from dc-dc converter
DEM_GND	38		Demodulator ground
DEM_VCC	40		Demodulator supply voltage
DET_OUT	45	O	Brownout detector output; active high
DGND	28		Digital ground
DVDD	17		Digital power supply
GND	42		Substrate ground
IF_IN1	44	I	Limiter amplifier noninverting input
IF_IN2	43	I	Limiter amplifier inverting input
LEARN/HOLD	39	I	Data slicer switch. Controls data slicer reference level
LNA_IN1	1	I	LNA noninverting input
LNA_IN2	2	I	LNA inverting input
LNA_VCC	3		LNA power supply
LPF_IN	37	I	Low-pass filter amplifier input
LPF_OUT	36	O	Low-pass filter amplifier output
MIX_GND	46		Mixer ground
MIX_OUT	47	O	Mixer output
MIX_VCC	48		Mixer supply voltage
MODE	21	I	Mode select input
PA_GND1	5		Power amplifier ground
PA_GND2	7		Power amplifier ground
PA_OUT	4	O	Power amplifier output
PA_VCC	6		Power amplifier supply voltage
RSSI_OUT	41	O	RSSI output signal
RX_DATA	33	O	Demodulated digital RX data
SLC_CAP	34		External capacitor for data slicer
$\overline{\text{STDBY}}$	26	I	Standby input signal; active low
STROBE	19	I	Serial interface strobe signal
TX_DATA	32	I	Buffered TX data input
VCO	11	I	VCO tank circuit connection
VCO_GND1	8		VCO ground
VCO_GND2	12		VCO ground
VCO_TUNE	13	I	Tuning voltage for the integrated VCO
VCO_VCC	9		VCO supply voltage
VCO_VCC2	10		VCO core supply voltage
XTAL	30	I/O	Connection to an external crystal
XTAL_SW	31	I	Connector to external capacitor which sets the frequency deviation of the transmitted signal
XTAL_VCC	29		Oscillator supply voltage

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range . . . . . –0.6 to 4.5 Vdc
Input voltage, logic signals . . . . . –0.6 to 4.5 Vdc
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
ESD protection, human body model (HBM) . . . . . 2 kV

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog supply voltage		1.8		3.6	V
Digital supply voltage		1.8		3.6	V
Operating free-air temperature		–40		85	°C

dc electrical characteristics over full range of operating conditions, V_{CC} = 2.7 V, T_A = 25°C

supply current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Standby current				0.6	4	µA
RX current				18	21	mA
TX current	0-dB attenuation‡			32	40	mA
	10-dB attenuation			27		
	20-dB attenuation			26		

‡ The TX current consumption is dependent upon the external PA matching circuit. The matching network is normally designed to achieve the highest output power at the 0-dB attenuation setting. Changing the external matching components to optimize the output power for other attenuation settings alters the typical current consumption from the typicals noted.

digital interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		V_{DD}–0.4		V_{DD}	V
V_{IL}	Low-level input voltage		0		0.4	V
V_{OH}	High-level output voltage	I_{OH} = 0.5 mA	V_{DD}–0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 0.5 mA			0.4	V
	Digital input leakage current			<0.01		µA

ac electrical characteristics over full range of operating conditions, V_{CC} = 2.7 V, T_A = 25°C

receiver (LNA, mixer, limiter, demod, LPF amplifier, data slicer, VCO, and PLL)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RX wake-up time				1	ms
BER	860 MHz to 930 MHz, IF = 10.7 MHz, BW = 280 kHz FSK deviation: ±32 kHz Bit rate: 19.2 kbit/s $-103 < P_{RFIN}$ (dBm) < -30		10^{-3}		

LNA/mixer

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Conversion gain			18		dB
SSB noise figure	Includes external matching network		6.5		dB
Input 1-dB compression point			–31		dBm
Input IP3			–19		dBm

IF/limiter amplifier

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			10.7		MHz
Voltage gain			86		dB
Noise figure	IF frequency = 10.7 MHz		4		dB

VCO

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency range—Europe	High-side injection	860		890	MHz
Frequency range—US	Low-side injection	890		930	MHz
Closed loop phase noise	Frequency offset = 50 kHz		–77		dBc/Hz
	Frequency offset = 200 kHz		–90		
Tuning voltage		0.1		V_{CC} at terminal 10	V

RSSI

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic range			70		dB
Rise time	R_L = 100 kΩ, C_L = 10 pF		2	3	µs
Slope			20		mV/dB
RSSI output current	R_L = 100 kΩ, C_L = 10 pF		30		µA

impedances and loads

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LNA_IN			See Figure 3		
MIX_OUT†			1400		Ω
IF_IN†	Differential		2600		Ω
PA_OUT			See Figure 9		

† Does not include external matching network.

ac electrical characteristics over full range of operating conditions, V_{CC} = 2.7 V, T_A = 25°C (continued)

transmitter (XTAL, PLL, VCO, and PA)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TX frequency range		860		930	MHz
Output power†	0-dB attenuation		9		dBm
	10-dB attenuation		0		
	20-dB attenuation		–10		
	Off‡		–50		
Output power (V_{CC} = 1.8 V)†	0-dB attenuation		6		dBm
	10-dB attenuation		–3		
	20-dB attenuation		–9		
Second harmonic			–15		dBc
Third harmonic			–20		dBc
Frequency deviation§	FSK		±32		kHz
Power ON-OFF ratio	OOK, 0-dB mode		50		dB
Data rate	FSK			64	kbit/s

† Matched to 50 Ω using external matching network.
‡ Not selectable with PA attenuation bits A<7:6>. Measured while the TRF6901 device is in RX mode.
§ Dependant upon external circuitry.

XTAL

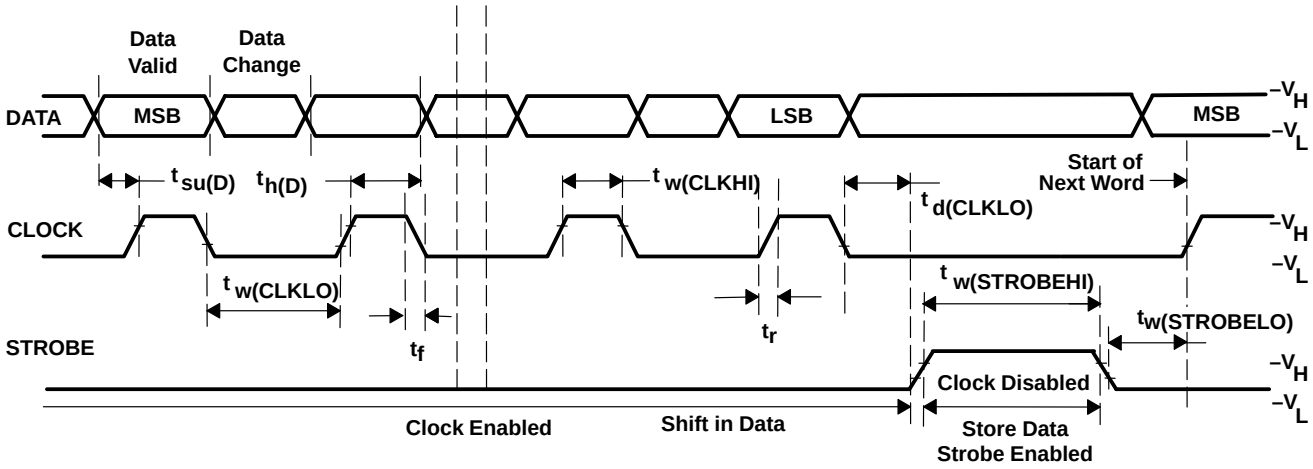
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency range		10		20	MHz

brownout detector

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage threshold, Vdet	Set by B<2:1>	1.8		2.4	V
Voltage steps (ΔV)			200		mV
Number of steps			4		
Output level	Connected to typical input port of microcontroller		CMOS		

timing data for serial interface

PARAMETER		MIN	MAX	UNIT
$f_{(CLOCK)}$	Clock frequency		20	MHz
$t_{w(CLKHI)}$	Clock high-time pulse width, clock high	25		ns
$t_{w(CLKLO)}$	Clock low-time pulse width, clock low	25		ns
$t_{su(D)}$	Setup time, data valid before CLOCK↑	25		ns
$t_{h(D)}$	Hold time, data valid after CLOCK ↑	25		ns
$t_{d(CLKLO)}$	Delay time of CLOCK low before STROBE high	25		ns
$t_{w(STROBEHI)}$	STROBE high-time pulse width, STROBE high	25		ns
$t_{w(STROBELO)}$	STROBE low-time pulse width, STROBE low	25		ns



NOTE: Most significant bit (MSB) clocked in first to the synthesizer.

Figure 2. Timing Data for Serial Interface

detailed description

low-noise amplifier (LNA)/RF mixer

The LNA has differential inputs. The off-chip input matching network has the dual task of matching a 50-Ω connector (or antenna, switch, filter, etc.) to the differential inputs and providing a 180-degree phase shift between the inputs at terminals 1 and 2. The differential input impedance of the LNA is approximately 500 Ω in parallel with 0.7 pF. The predicted noise figure of the LNA and input matching circuit is 2.5 dB. The cascaded noise figure for the LNA/mixer is listed in the specifications.

The mixer offers good linearity (high IP3). An external matching network is required to transform the output impedance of the mixer (1.4 kΩ) to the input impedance of the IF filter (typically 330 Ω).

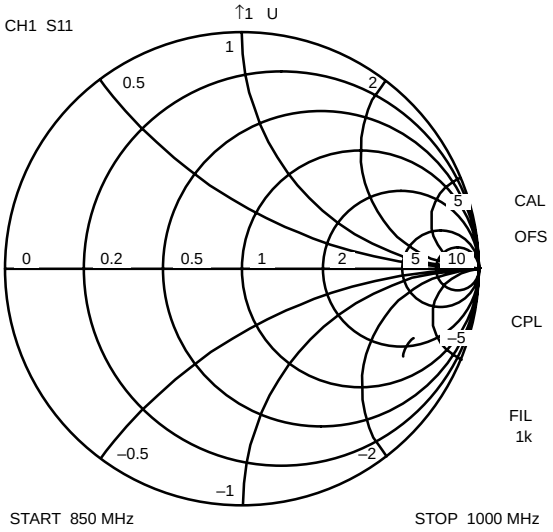


Figure 3. Typical LNA Input Impedance (S11) at Device Terminals LNA_IN1,2

IF amplifier/limiter

The IF amplifier has differential inputs to its first stage. The limiting amplifier provides 68 dB of gain. An external impedance matching network is required between the IF filter output and the IF amplifier inputs at terminals 43 and 44.

RSSI

The received signal strength indicator (RSSI) voltage at terminal 41 is proportional to the log of the down-converted RF signal at the IF limiting amplifier input. The RSSI circuit is temperature compensated and is useful for detecting interfering signals, transceiver handshaking, and RF channel selection. In some applications it can be used as a demodulator for amplitude-shift\keying (ASK) or on-off keying (OOK) modulation.

detailed description (continued)

demodulator

The quadrature demodulator decodes digital frequency shift keying (FSK) modulation. An external ceramic discriminator or an equivalent discrete circuit is required at terminal 35. The demodulator is optimized for use with a ceramic discriminator. Thus, the use of a packaged ceramic discriminator is recommended for the best performance. Internal resistors can be programmed with D<14:12> to tune the demodulator center frequency. The recommended default setting for the demodulator tuning bits is D<14:12> = 110. The resonant frequency of the discrete-component discriminator can be calculated from the inductor and capacitor values used in the circuit. A parallel resistor may be added to reduce the quality factor (Q) of the tank circuit, depending on the application.

$$f_{res} = \frac{1}{2\pi\sqrt{LC}}$$

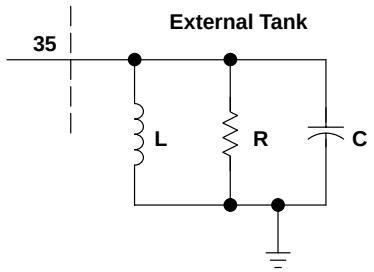


Figure 4. Optional External Discrete Demodulator Tank

post-detection amplifier/low-pass filter

The post-detection amplifier operates as a low-pass transimpedance amplifier. The external low-pass filter circuit must be optimized for the data rate. The 3-dB corner frequency of the low-pass filter should be greater than twice the data rate. Various low-pass filter designs use two to five components and may be first- or second-order designs. Simple 2-element filter component values and 3-dB bandwidths are contained in Table 1.

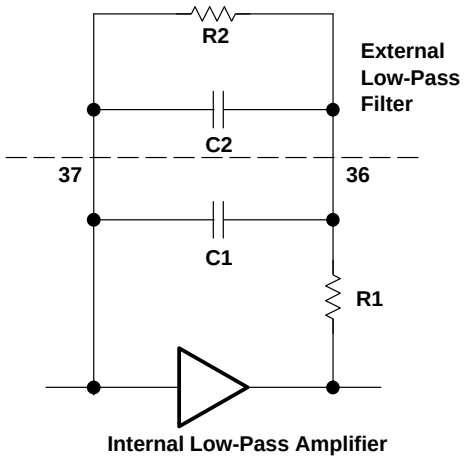


Figure 5. Post-Detection Amplifier/Low-Pass Filter

Table 1. Various Post-Detection Amplifier/Low-Pass Filter 3-dB Bandwidth and Corresponding Component Values

f_{3dB} (kHz)	10	20	30	60
R2 (kΩ)	220	220	220	220
C2 (pF)	68	33	22	10

detailed description (continued)

data slicer

The data slicer is a comparator circuit for received digital (FSK) data. The data slicer output voltage depends on the difference between the received signal and a reference voltage (at the sample-and-hold (S&H) capacitor) used as a decision threshold. During the learn mode, the S&H capacitor connected to terminal 34 is charged up to the average dc voltage of a training sequence of alternating ones and zeroes; this establishes the reference voltage to be used as a decision level before a sequence of actual data is received in the hold mode. During long data transmissions, more training sequences may be necessary to recharge the S&H capacitor.

If the modulation scheme is dc-free (Manchester coding) or constant-dc, the TRF6901 may be operated continuously in the learn mode, and no training sequence is necessary before the transmission of a data string. However, the S&H capacitor voltage may be incorrect during power up or after long periods of inactivity (no data transmission); a learning sequence before each data transmission is recommended.

The comparator is a CMOS circuit that does not load the S&H capacitor, so leaving the transmission gate (learn/hold switch) open during periods of inactivity may be useful in maintaining the capacitor reference voltage; however, it gradually discharges due to leakage current.

The time constant for charging the S&H capacitor is determined by its capacitance and an internal 50-kΩ resistor. A slow data rate requires a larger S&H capacitor (longer time constant). The value of the S&H capacitor, Csh, can be calculated with the following equation:

$$Csh \cong \frac{5 \times T}{50000}$$

where T is the bit period.

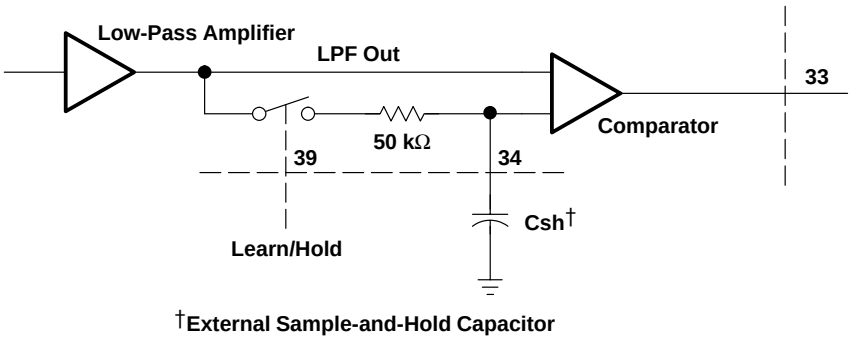


Figure 6. Data Slicer

main divider

The main divider is composed of a 5-bit A-counter, a 9-bit B-counter, and a prescaler. The A-counter controls the divider ratio of the prescaler, which divides the VCO signal by either 33 or 32. The prescaler divides by 33 until the A-counter reaches its terminal count and then divides by 32 until the B-counter reaches terminal count, whereupon both counters reset and the cycle repeats. The total divide-by-N operation is related to the 32/33 prescaler by:

$N_{TOTAL} = 33 \times A + 32 \times (B - A)$

where $0 \le A \le 31$ and $31 \le B \le 511$ or, $N_{TOTAL} = A + 32B$

Thus, the N-divider has a range of $992 \le N_{TOTAL} \le 16383$.

detailed description (continued)

PLL

The phase-locked loop is the radio frequency synthesizer for the TRF6901. It is used to generate the transmit signal and as the local oscillator for the receive mixer. The signal (F_X) from a reference crystal oscillator (XO) is divided by an integer factor R down to F_R. The minimum frequency resolution, and thus, the minimum channel spacing, is F_R.

$F_R = F_X \div R$, where $1 \le R \le 256$

The phase-locked loop is an integer-N design. The voltage-controlled oscillator (VCO) signal is divided by an integer factor N to get a frequency at the phase detector input.

$F_{PD} = F_{VCO} \div N$, where $F_{VCO} = F_{OUT}$

The phase detector compares the divided VCO signal to the divided crystal frequency and implements an error signal from two charge pumps. The error signal corrects the VCO output to the desired frequency.

With $F_R = F_{PD}$ under locked conditions, $F_{OUT} = \frac{F_X N}{R} = (A + 32B)\, F_R$.

As is in any integer-N PLLs, the VCO output has spurs at integer multiples of the reference frequency (nF_R). In applications requiring contiguous frequency channels, the reference frequency is often chosen to be equal to the channel spacing, thus, channel spacing = $F_R = F_X \div R$.

oscillator circuit and reference divider

The reference divider reduces the frequency of the external crystal (F_X) by an 8-bit programmable integer divisor to an internal reference frequency (F_R) used for the phase-locked loop. The choice of internal reference frequency also has implications for lock time, maximum data rate, noise floor, and loop-filter design. The crystal frequency can be tuned using the D word to control internal trimming capacitors, which are placed in parallel with the crystal. These offset a small frequency error in the crystal. In an FSK application, an additional capacitor is placed in parallel (through terminal 31) with the external capacitor that is connected in series with the crystal, thus, changing the load capacitance as the transmit data switch (TX_DATA, terminal 32) is toggled. The change in load capacitance pulls the crystal off-frequency by the total frequency deviation.

Hence, the 2-FSK frequency set by the level of TX_DATA and the external capacitor, can be represented as follows:

f_{out1} = TX_DATA Low $\qquad\qquad$ f_{out2} = TX_DATA High

Note that the frequencies f_{out1} and f_{out2} are centered about the frequency $f_{center} = (f_{out1} + f_{out2})/2$. When transmitting FSK, f_{center} is considered to be the effective carrier frequency and any receiver local oscillator (LO) should be set to the same f_{center} frequency $\pm$ the receiver's IF frequency (f_{IF}) for proper reception and demodulation.

For the case of high-side injection, the receiver LO would be set to $f_{LO} = f_{center} + f_{IF}$. Using high-side injection, the received data at terminal 33, RX_DATA, would be inverted from the transmitted data applied at terminal 32, TX_DATA. Conversely, for low-side injection, the receiver LO would be set to $f_{LO} = f_{center} - f_{IF}$. Using low-side injection, the received data would be the same as the transmitted data.

In addition, when the TRF6901 is placed in receive mode, it is recommended that the TX_DATA terminal be kept low. In this manner, the actual LO frequency injected into the mixer is $f_{out1} = f_{LO}$. If TX_DATA is set high, the the receiver LO would be offset, resulting in poor receiver sensitivity.

detailed description (continued)

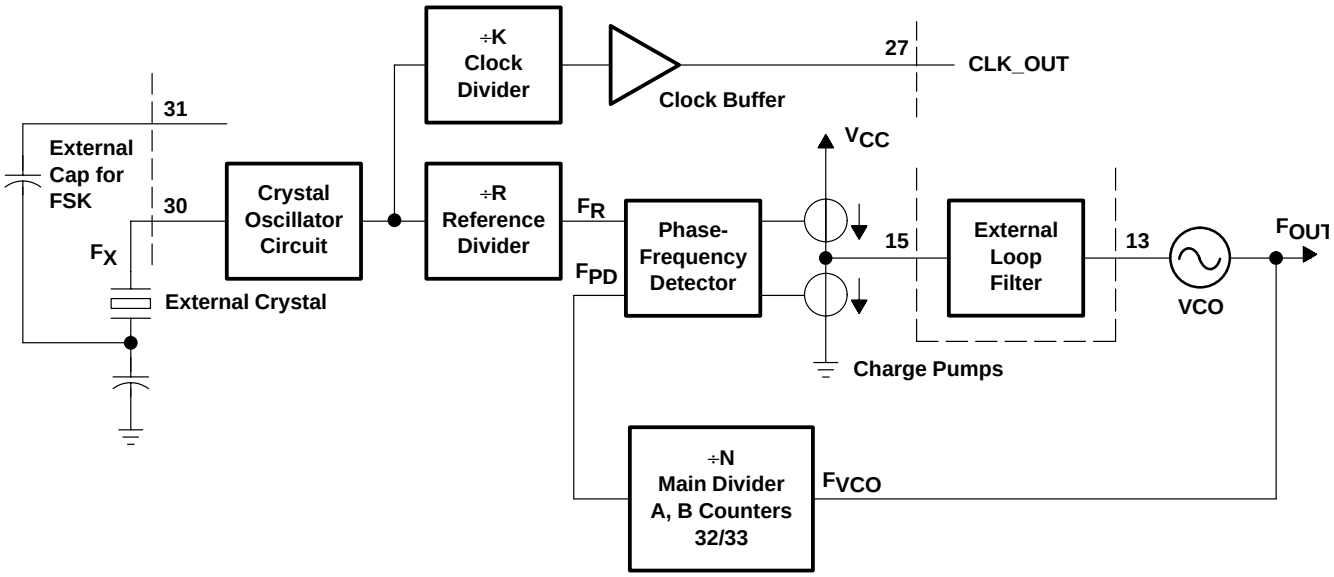


Figure 7. TRF6901 PLL and Clock Divider

phase detector and charge pumps

The phase detector is a phase-frequency design. The phase-frequency detector gain is given by:

$$K_P = I_{(CP)}/2\pi$$

where, $I_{(CP)}$ is the peak charge pump current. The peak charge pump current is programmable with A<4:2> in three steps: 250 μA, 500 μA, and 1000 μA.

loop filter

The loop filter must be carefully chosen for proper operation of the TRF6901. The loop filter is typically a second- or third-order passive design and in FSK operation should have a bandwidth wide enough to allow the PLL to relock quickly as the external crystal frequency is pulled off-center during modulation. The loop filter should also be wider than the data modulation rate. These requirements should be balanced with making the loop narrow enough in consideration of the reference frequency. In OOK the VCO frequency is not changed during data modulation, so the filter bandwidth may be narrower than the modulation bandwidth. Filters can be calculated using standard formulas in reference literature. Some third-order filter examples are shown in Table 2.

$$F(s) = \frac{1 + sC2R2}{s(C1 + C2 + sC1C2R2)} \times \frac{\frac{1}{C3R3}}{s + \frac{1}{C3R3}}$$

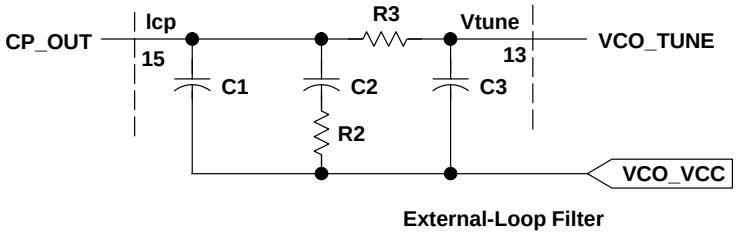


Figure 8. Third-Order Loop Filter and Transfer Function

loop filter (continued)

Table 2. Various Loop Filter Nat Freq Component Pole Values and Corresponding Bandwidths

3 dB BW (kHz)	REF Freq (kHz)	Icp (mA)	3rd Pole (kHz)	C1 (pF)	R2 (kΩ)	C2 (nF)	R3 (kΩ)	C3 (pF)
10.4	100	0.5	100	1590	7	15.9	10	159
20	100	0.5	100	440	13.2	4.4	36	44
10.4	200	0.5	100	3200	3.5	31.8	5	320
20	200	0.5	100	880	6.6	8.8	18	88
20	200	0.5	200	880	6.6	8.8	9	88
30	200	0.5	100	390	9.9	3.9	40	39
20	400	0.5	200	1740	3.3	17.4	4.6	170
30	400	0.5	200	780	5	7.8	10	78
40	400	0.5	200	430	6.8	4.2	18.7	42

VCO

The voltage-controlled oscillator (VCO) produces an RF output signal with a frequency that is dependant upon the dc-tuning voltage at terminal 13. The tank circuit is passive and has integrated varactor diodes and inductors. The VCO has an open-loop operating band from approximately 700 MHz to 1 GHz. The open-loop VCO gain is approximately 100 MHz/V.

power amplifier

The power amplifier has four programmable output states: full power, 10-dB attenuation, 20-dB attenuation, and off (receive mode). The output s-parameters of the amplifier may change slightly as the bias point is changed. During receive, the transmit power amplifier is powered down but the VCO is still operating. During ASK or OOK operation, the TX_DATA signal turns the power amplifier on and off according to the transmit data incident at terminal 32.

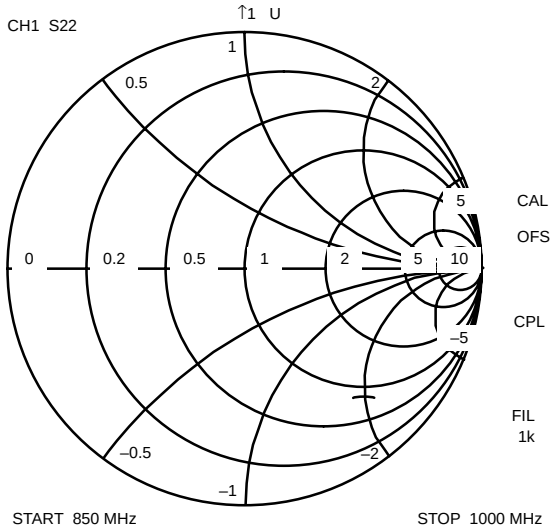


Figure 9. Typical PA Output Impedance (S22) at Device Terminal PA_OUT

detailed description (continued)

dc-dc converter

The dc-dc converter provides an adequate voltage to the charge pumps and VCO core in the event the power supply voltage drops down to 1.8 V. The switching frequency is adjustable through a clock divider that reduces the external clock frequency by a C-word programmable factor (L) of 2 to 254 in steps of 2. The dc-dc converter is designed to operate at a switching frequency of around 1 MHz, so a suggested divider ratio to use with a 20-MHz crystal frequency is 16 or 32 (C<6:0>). The power supply to terminals 10 and 16 may be from Vcc (regulated supply or battery) or from the dc converter output at terminal 22, but not both. Operation at a reduced supply voltage is possible without the dc-dc converter if there is adequate VCO tuning voltage overhead at the highest and lowest frequencies of operation. The dc-dc converter makes operation at low supply voltages (around 1.8 V) possible, where there would otherwise be insufficient overhead to operate the VCO core and charge pumps.

brownout detector

The brownout detector provides an output voltage to indicate a low supply voltage. This may be used to signal the need to change transmit power to conserve battery life, or for system power down. The brownout detector threshold is set with the B word. Four different thresholds are available.

clock-output buffer

The clock-output buffer is provided to use the TRF6901 crystal oscillator to drive an external microcontroller (MCU) or other baseband device, eliminating the need for a second clock circuit. A divider reduces the external crystal frequency by a C-word programmable integer factor (K) of 2 to 62 in steps of 2. It is recommended that the clock output buffer divider (C<12:8>) be a power of two, i.e., 2, 4, 8, 16, etc. A buffer amplifier provides adequate drive for an external MCU, FPGA, or DSP. When the transmit section of the TRF6901 is operated in FSK, the crystal frequency, internal reference frequency, and the output buffer frequency are modulated by the total frequency deviation as the transmit data switch is toggled. The resulting MCU clock jitter should be acceptable for baseband applications. It is possible to run the TRF6901 from an external clock oscillator circuit by an overdriving signal at terminal 30; however, in FSK the external clock circuit must be modulated. When the TRF6901 is in standby, the clock buffer output at terminal 27 is turned off.

serial control interface

The TRF6901 is controlled through a serial interface; there are four 24-bit control words (A, B, C, D) which set the device state. The A and B words are almost identical and provide configuration settings for two modes, designated 0 and 1, which are commonly used to configure the transmit and receive states. The transmit and receive states can then be rapidly selected using MODE (terminal 21). The C word sets the various clock dividers. The D word is used to trim the external crystal frequency and tune the demodulator.

PRINCIPLES OF OPERATION

register description

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	Address																							
A	0	0	Main A-Divider Coefficient (Mode 0)					Main B-Divider Coefficient (Mode 0)									PA		TX/ RX	0	CP Acc.		0	dc-dc
B	0	1	Main A-Divider Coefficient (Mode 1)					Main B-Divider Coefficient (Mode 1)									PA		TX/ RX	FSK/ OOK	Buf	Detector Threshold		Det. Enable
C	1	0	Reference Divider Coefficient								0	Buffer Clock Divider Coefficient					0	dc-dc Clock Divider Coefficient						
D	1	1	0	0	0	XTAL_Tune			PFD reset	Dem_Tune			0	0	0	0	0	0	0	0	0	0	0	0

ADDRESS		BITS	DESCRIPTION
00	21:17	5	Main A-divider coefficient (Mode 0)
00	16:8	9	Main B-divider coefficient (Mode 0)
00	7:6	2	Controls the PA attenuation (Mode 0)
00	5	1	Enables transmit/receive path (Mode 0)
00	3:2	2	Controls speed up time for the charge pumps (Mode 0)
00	1	1	Set to 0
00	0	1	Enables the dc-dc converter
01	21:17	5	Main A-divider coefficient (Mode 1)
01	16:8	9	Main B-divider coefficient (Mode 1)
01	7:6	2	Controls the PA attenuation (Mode 1)
01	5	1	Enables transmit/receive path (Mode 1)
01	4	1	Controls modulation scheme (FSK or OOK)
01	3	1	Enables the XTAL output buffer
01	2:1	2	Sets threshold for the brownout detector
01	0	1	Enables brownout detector
10	21:14	8	Reference divider coefficient
10	12:8	5	Buffer clock divider coefficient (K-divider)
10	6:0	7	DC-DC converter clock divider coefficient (L-divider)
11	18:16	3	Tunes the XTAL frequency by using an internal capacitor bank
11	15	1	PFD reset
11	14:12	3	Tunes the resonant frequency of the external demodulation tank circuit

At power on/startup, all of the TRF6901 register contents are zero, with the exception of the power amplifier attenuation registers and the phase-frequency detector reset register. The power amplifier attenuation registers are set to zero attenuation, i.e., A<7:6>=10 and B<7:6>=10. The PFD reset register is set to the prescaler setting, i.e., D<15>=1.

PRINCIPLES OF OPERATION

Address 00 (A-Word)

Terminal 21 (MODE) selects bits A<21:5> if low, or B<21:5> if high.

Main divider A<21:17>: 5-bit value for divider ratio of the A-counter
Main divider A<16:8>: 9-bit value for divider ratio of the B-counter
PA attenuation A<7:6>: 2 bits for setting the PA attenuation

A<7:6>	PA ATTENUATION
00	10 dB
01	20 dB
10	0 dB
11	Not defined

A<5>: 1 bit TX/RX mode select

A<5>	TX/RX MODE
0	RX mode
1	TX mode

A<3:2>: 2 bits for setting the charge pump current

A<3:2>	CP CURRENT
00	0.5 mA
01	1 mA
10	0.25 mA
11	Not defined

A<1>: Set to 0

A<0>: Enables or disables the dc-dc converter

A<0>	DC-DC CONVERTER
0	Off
1	On

NOTE: When A<0> is high, at least one bit in C<6:0> must be high to enable the VCO.

Address 01 (B-Word)

Terminal 21 (MODE) selects bits A<21:5> if low, or B<21:5> if high.

Main divider B<21:17>: 5-bit value for divider ratio of the A-counter
Main divider B<16:8>: 9-bit value for divider ratio of the B-counter
PA attenuation B<7:6>: 2 bits for setting the PA attenuation

B<7:6>	PA ATTENUATION
00	10 dB
01	20 dB
10	0 dB
11	Not defined

B<5>: 1 bit TX/RX mode select

B<5>	TX/RX MODE
0	RX mode
1	TX mode

B<4> 1 bit modulation select

B<4>	MODULATION
0	OOK
1	FSK

B<3>: 1 bit to enable terminal 27 (reference clock buffer)

B<3>	REFERENCE CLOCK BUFFER
0	Off
1	On

NOTE: If C<12:8> are all low, the reference clock buffer is disabled independent of B<3>.

B<2:1>: 2-bit value to set the threshold voltage for the brownout detector

B<2:1>	VOLTAGE
00	1.8 V
01	2 V
10	2.2 V
11	2.4 V

B<0>: 1 bit to enable brownout detector

B<0>	BROWNOUT DETECTOR
0	Off
1	On

PRINCIPLES OF OPERATION

Address 10 (C-Word)

Reference divider C <21:14>: 8-bit value for divider ratio of reference divider. The allowable reference divider range is 2 (C <21:14> = 00000010) through 255 (C <21:14> = 11111111).
Buffer clock divider C <12:8>: 5-bit value for divider (K-divider) for the buffer clock for an external microcontroller.

C<12:8>	BUFFER CLOCK DIVIDE FACTOR
00000	Clock output buffer off
00001	2
00010	4
00011	6
00100	8
00101	10
00110	12
00111	14
01000	16
01001	18
01010	20
01011	22
01100	24
01101	26
01110	28
01111	30
10000	32
10001	34
10010	36
10011	38
10100	40
10101	42
10110	44
10111	46
11000	48
11001	50
11010	52
11011	54
11100	56
11101	58
11110	60
11111	62

NOTE:

C<12> is the MSB and C<8> is the LSB. The microcontroller clock divider is followed internally by a divide-by-2 stage to achieve a 50% duty cycle. This additional division is not included in the 5-bit setting. The maximum valid divider factor is 62. The minimum valid divider factor is 2. The clock buffer output frequency must be set to an integer multiple of the reference frequency by the buffer clock divide factor.

Address 10 (C-Word) (continued)

dc-dc clock divider C <6:0>: 7-bit value for divider (L-divider) for setting the dc-dc converter clock divider

C<6:0>	DC–DC CLOCK DIVIDE FACTOR
0000000	When A<0> is high and C<6:0> are all low, the VCO shuts off. At least one bit in C<6:0> must be set high to enable the VCO.
0000001	2
0000010	4
0000011	6
0000100	8
0000101	10
0000110	12
0000111	14
0001000	16
0001001	18
0001010	20
0001011	22
0001100	24
0001101	26
0001110	28
0001111	30
0010000	32
0010001	34
0010010	36
0010011	38
0010100	40
0010101	42
0010110	44
0010111	46
0011000	48
0011001	50
0011010	52
0011011	54
0011100	56
0011101	58
0011110	60
0011111	62
0100000	64
0100001	66
0100010	68
0100011	70
0100100	72
0100101	74
0100110	76
0100111	78
0101000	80

Address 10 (C-Word) (continued)

C<6:0>	DC–DC CLOCK DIVIDE FACTOR
0101001	82
0101010	84
0101011	86
0101100	88
0101101	90
0101110	92
0101111	94
0110000	96
0110001	98
0110010	100
0110011	102
0110100	104
0110101	106
0110110	108
0110111	110
0111000	112
0111001	114
0111010	116
0111011	118
0111100	120
0111101	122
0111110	124
0111111	126
1000000	128
1000001	130
1000010	132
1000011	134
1000100	136
1000101	138
1000110	140
1000111	142
1001000	144
1001001	146
1001010	148
1001011	150
1001100	152
1001101	154
1001110	156
1001111	158
1010000	160
1010001	162
1010010	164
1010011	166
1010100	168
1010101	170

C<6:0>	DC–DC CLOCK DIVIDE FACTOR
1010110	172
1010111	174
1011000	176
1011001	178
1011010	180
1011011	182
1011100	184
1011101	186
1011110	188
1011111	190
1100000	192
1100001	194
1100010	196
1100011	198
1100100	200
1100101	202
1100110	204
1100111	206
1101000	208
1101001	210
1101010	212
1101011	214
1101100	216
1101101	218
1101110	220
1101111	222
1110000	224
1110001	226
1110010	228
1110011	230
1110100	232
1110101	234
1110110	236
1110111	238
1111000	240
1111001	242
1111010	244
1111011	246
1111100	248
1111101	250
1111110	252
1111111	254

NOTE:

C<6> is the MSB and C<0> is the LSB. The dc-dc clock divider is followed internally by a divide-by-2 stage to achieve a 50% duty cycle. This additional division is not included in the 7-bit setting. The maximum valid divider factor is 254. The minimum valid divider factor is 2.

PRINCIPLES OF OPERATION

The dc-dc clock divide factor should be chosen such that the resultant dc-dc converter switching frequency is between 150 kHz and 1000 kHz.

Address 11 (D-Word)

D<18:16>: 3-bit value to fine-tune the XTAL frequency by using an internal capacitor bank

D<18:16>	TYPICAL LOAD CAPACITANCE
000	13.23 pF
001	22.57 pF
010	17.9 pF
011	27.24 pF
100	15.56 pF
101	24.9 pF
110	20.23 pF
111	29.57 pF

D<15>: 1-bit value to select the reset signal for the PFD

D<15>	RESET SIGNAL
0	Derived from XTAL
1	Derived from prescaler

NOTE: The default setting for D<15> is 1.

D<14:12>: 3-bit value to tune the resonant frequency of the external demodulator tank circuit. It can be used to optimize the receiver performance. The recommended default setting is 110.

PRINCIPLES OF OPERATION

operating modes

Controlled with terminal 26, $\overline{\text{STDBY}}$

$\overline{\text{STDBY}}$	OPERATING MODE
0	Power down of all blocks—programming mode
1	Operational mode

Controlled with terminal 21, MODE

MODE	OPERATING MODE
0	Enable A-word
1	Enable B-word

Controlled with terminal 39, LEARN/HOLD

LEARN/HOLD	OPERATING MODE
0	Selects data slicer decision level to HOLD
1	Selects data slicer decision level to LEARN

APPLICATION INFORMATION

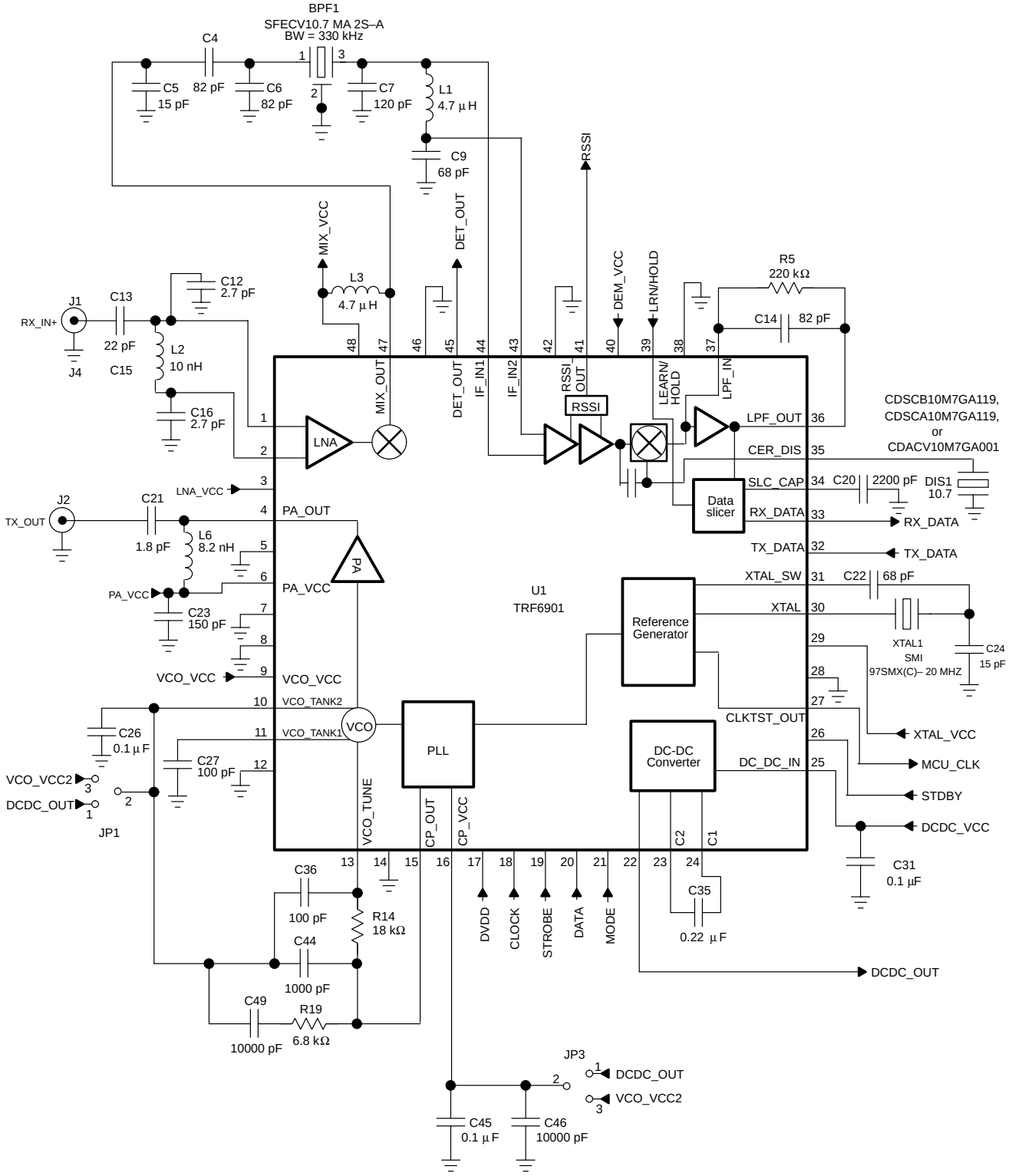


Figure 10. Typical Application Schematic for the 868-MHz to 870-MHz European ISM Band 32-kbps NRZ, ±50-kHz Deviation FSK Application

APPLICATION INFORMATION

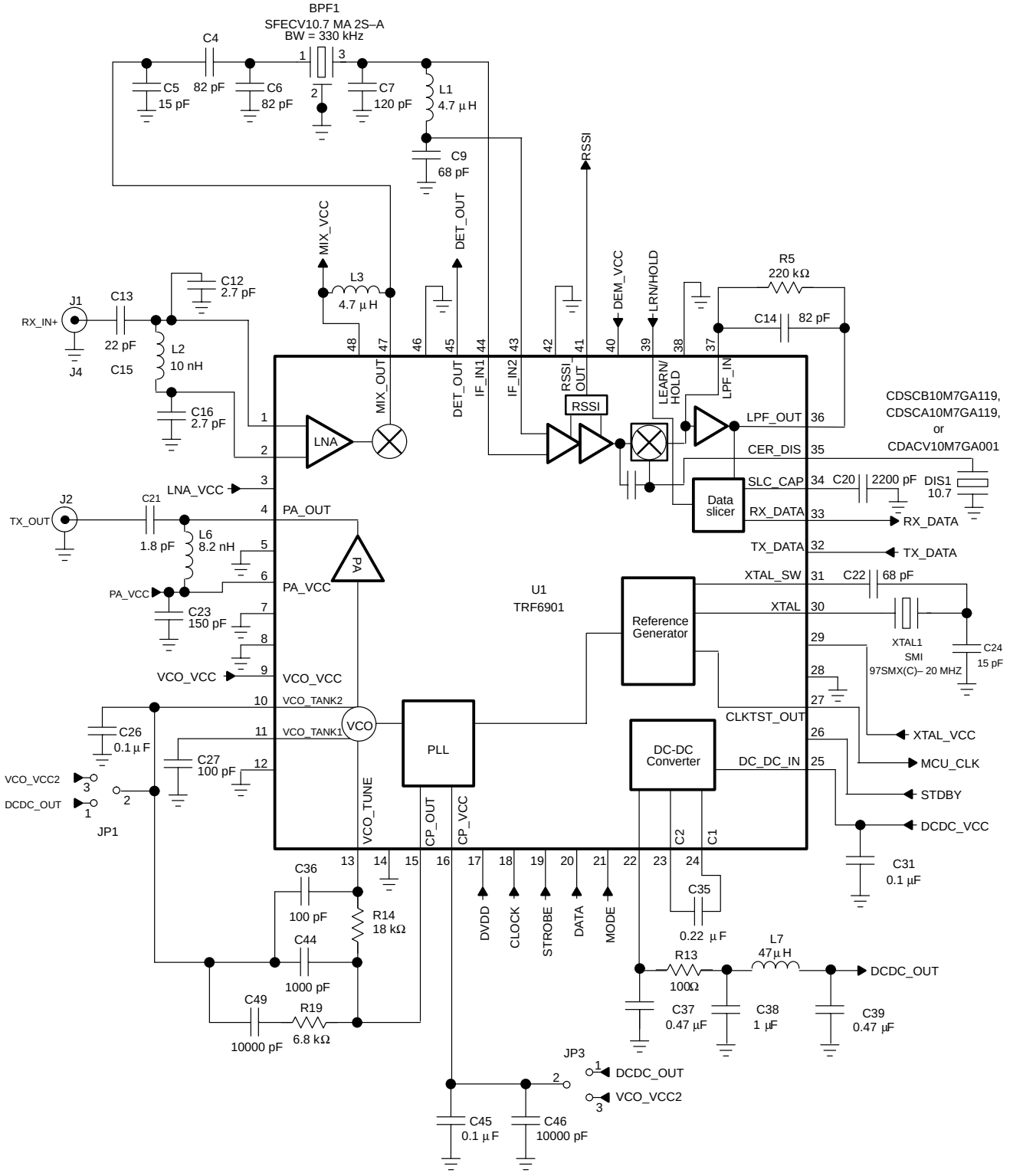
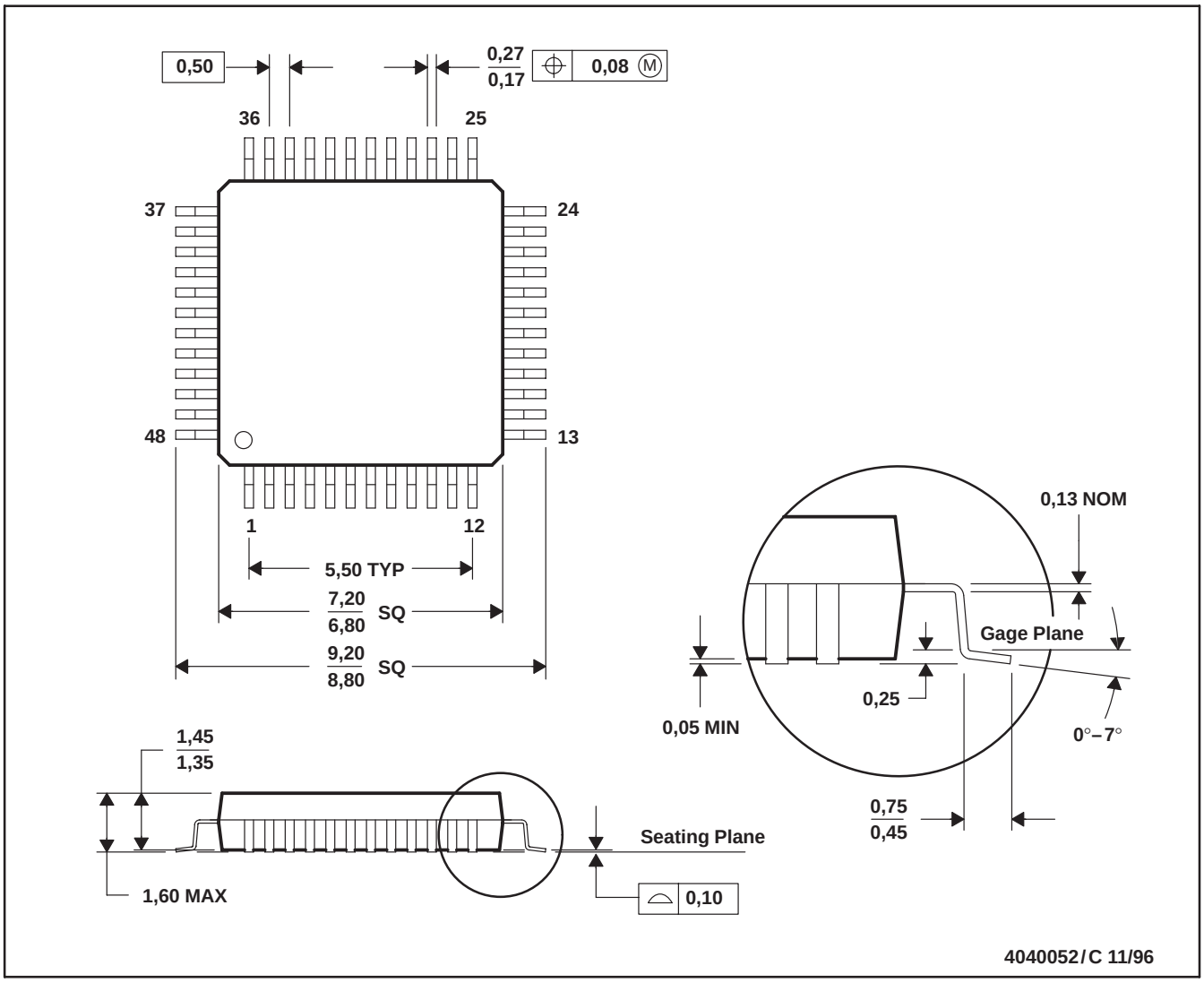


Figure 11. Typical Application Schematic for the 902-MHz to 928-MHz North American 32-kbps NRZ, ±50-kHz Deviation FSK Application

MTQF003A – OCTOBER 1994 – REVISED DECEMBER 1996

PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. This may also be a thermally enhanced plastic package with leads conected to the die pads.

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